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Single-event effects: experimental setup for power MOSFETs and diffusion model for cross section calculations in low-voltage MOSFETs

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Abstract. MOSFETs are subject to different types of Single-Event Effects (SEEs) induced by heavy ions, with low-voltage MOSFETs being more susceptible to non-destructive effects, such as Single-Event Transients, than high-voltage MOSFETs which may also be susceptible to destructive effects. In this paper an experimental setup used to study SEEs in power MOSFETs at the São Paulo 8UD Pelletron accelerator and computational simulations for SEE cross section calculations in low-voltage MOSFETs are presented.

1. Introduction

Since the mid 1970s, it is known that electronic devices are subject to operational failures when exposed to radiation [1, 2]. These operational failures are very significant in environments where the exposure to radiation is quite intense, such as satellites, avionic systems, particle accelerators, and nuclear reactors. Single-Event Effects (SEEs) are a class of ionizing radiation effects in electronic devices that has been dominant in embedded space systems [3]. SEEs are caused by the incidence of a single ionizing particle with enough energy to create a large number of electron-hole pairs within a sensitive volume of the electronic device. Under conduction and drift movements within the device, the electron-hole pairs configure electric currents that are able to cause non-destructive effects (soft errors) like electric transients in analog circuits (Single-Event Transient - SET), logical state changes in digital circuits (Single-Event Upset - SEU), and even destructive effects (hard errors). Although computational methods are able to estimate the radiation effects caused on electronic devices [4], any such devices should be able to withstand particle accelerator testing in order to be considered safe for use in space applications [5].

Currently, a beam line named SAFIIRA ("*SistemA de Feixes Iônicos para IRradiações e Aplicações*") dedicated to studies of SEEs with heavy ions was developed at the São Paulo 8UD Pelletron accelerator [6]. This experimental setup has been used to study the radiation effects in power MOSFETs which, in radiation environments, are liable to suffer soft errors, such as SETs, and hard errors, such as Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR) [7]. Recently, SET and SEB cross section measurements in power transistors were carried out using a non-destructive method for the ionic species available at the 8UD Pelletron accelerator and the data obtained are under analysis.

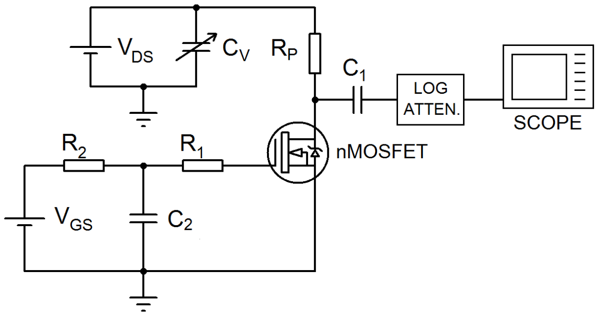

Figure 1. Schematic diagram of the test setup for SET, SEGR and protective SEB measurements.

In the first part of this paper we present a description of the experimental test setup that has been used for SEE studies in power MOSFETs. In this frame, the circuitry considerations are detailed in an updated perspective for accurate measurements. In the second part, a Monte Carlo routine based on a diffusion model for SEUs in memory devices was adapted to SETs in low-voltage MOSFETs and the results are shown.

2. Test Setup for MOSFET irradiation

The irradiation experiments in power MOSFETs has been conducted at SAFIIRA [6], located at the 8UD Pelletron accelerator of the "*Laboratório Aberto de Física Nuclear da Universidade de São Paulo*" (LAFN-USP, Brazil). SAFIIRA was designed in order to obtain low-intensity highly-uniform heavy ion beams in the device under test (DUT) through the combination of Rutherford scattering and quadrupole defocusing techniques. The 8UD Pelletron accelerator is able to provide ion beams from ^{1}H up to ^{107}Ag with a surface Linear Energy Transfer (LET) in silicon ranging from 0.5 to 40 MeV.mg^{-1}.cm^{-2}.

Power MOSFETs may be subject to different effects (mainly SET, SEB and SEGR) and to measure them an electric circuit was developed taking into account modern circuitry considerations [7, 8]. Although SEBs are entirely destructive events, protective methods based on the current limiting technique are well known and used for cross section measurements in the usual way [9, 10]. In Figure 1 the proposed test setup for the SEE measurements in power MOSFETs, including protective electric circuit and the acquisition system, is shown.

SEE qualifications should be performed considering the worst case, *i.e.*, under conditions that maximize the SEE cross section. For non-destructive SEB measurements, the value of the protection resistor R_P (Figure 1) is responsible for the effectiveness of the protective method and for the accuracy of the measures taken. An appropriate value of R_P can be estimated if the characteristic curve for the avalanche regime is known, which can be obtained by direct measurements or quasi-stationary avalanche simulations [8]. In the absence of the high-voltage characteristic curve, the value for R_P can be estimated if the DUT drain-to-source leakage current i_{DSS} is known, since, for high values of R_P, the voltage drop in the protection resistor is not negligible with respect to the voltage drop through the DUT and the V_{DS} applied [11].

In SEB measurements, the capacitor C_1 is charged by the power supply V_{DS} while the MOSFET remains in the off state ($V_{GS} = 0$ e $V_{DS} > 0$). SEB can be triggered if the heavy ion strike turns on the *npn* parasitic bipolar transistor for a certain critical voltage $V_{DS_{th}}$ and a second breakdown occurs. Since the equivalent impedance between the oscilloscope and the attenuator is 50 Ω, C_1 is discharged to provide current to the MOSFET due to the fact that the protection resistor R_P limits the current provided by the power supply V_{DS}. The nominal value of C_1 must be chosen in accordance with the particle flux on the DUT area and the desired signal detection time. Although the electric current provided by C_1 depends on its nominal value, higher values can provide a large amount o charge to destroy the DUT and disable the limiting current technique [10].

Traditionally, in SEB measurements a stiffening capacitor C_V is used, which is ideally placed as close as possible to the DUT. Is assigned to the capacitor C_V the function of filtering high frequency noises, compensating voltage drops to the DUT and minimizing parasitic circuit effects. However, it is expected that small ion-induced transients can occur while V_{DS} is low enough to trigger a SEB. In this case, C_V can suppress the transient detection by quickly compensating these voltage drops in the DUT and its usage is not recommended for SET cross section measurements.

The electric circuit also allows identification of SEGR if a picoammeter monitors the current provided by the power supply V_{GS}. The network R_1-C_2-R_2 is used as a suppression filter to prevent electrical stress in the gate oxide. Its use is exclusively preventive because, unlike protective SEB measurements, to the present day there are no protective methods for SEGR cross section measurements.

3. DMSEE: Diffusion Model for Single-Event Effect Cross Section Calculations

In the occurence of a SEE, the electron-hole pairs created in the plasma filament can be collected by a sensitive region of the device through diffusion and drift transport. In the particular case where the electric field intensity inside the device is low enough, the diffusion transport is predominant.

Wrobel's diffusion method [13] is based on the calculation of the total collected charge Q_c by a sensitive region of an electronic device considering the diffusion of each elemental ion track produced by the ion strike. Thus, the deposited charge at a point Z of the ion track, $Q_d(Z)$, is related to Q_c through the solid angle of the sensitive region viewed from point Z, denoted $\Omega(Z)$:

$$Q_c = Q_d(Z) \cdot \frac{\Omega(Z)}{4\pi} \tag{1}$$

The stopping power curves can be calculated for several ion species using the SRIM code [14] and a Monte Carlo routine simulates the ion beam incidence. In this method, the SEE cross sections are calculated using the critical charge criterion (or critical energy in silicon), i.e., a SEE occurs if Q_c exceeds a predefined critical value.

Based on Wrobel's method for SEU cross section calculations in memory devices [13], the DMSEE (Diffusion Model for Single-Event Effect cross section calculations) code was developed. DMSEE considers passivation and metallization layers of the device in its calculations and the solid angles are calculated for parallelepiped sensitive volumes by using analytical solutions rather than numerical approaches [15].

To explore DMSEE applications, a low-voltage pMOSFET, whose sensitive area and critical charge can be easily estimated (from reference [16]), was simulated. The sensitive volume size and the critical energy were estimated to be about $50\times50\times1$ μm^3 and 11 MeV, respectively. In addition, 1 μm passivation (SiO_2) and metallization (Al) layers were considered. Figure 2 shows the geometry adopted and the resulting simulation.

The Weibull function shape could be obtained and the Weibull fit parameters resemble the experimental ones. As discussed in [13], the diffusion model is not able to perform predictions for LETs near the threshold. However, given the inaccurate estimates considered as input to DMSEE, this simplified methodology presents promising results and extends the application of Wrobel's method to SEUs only.

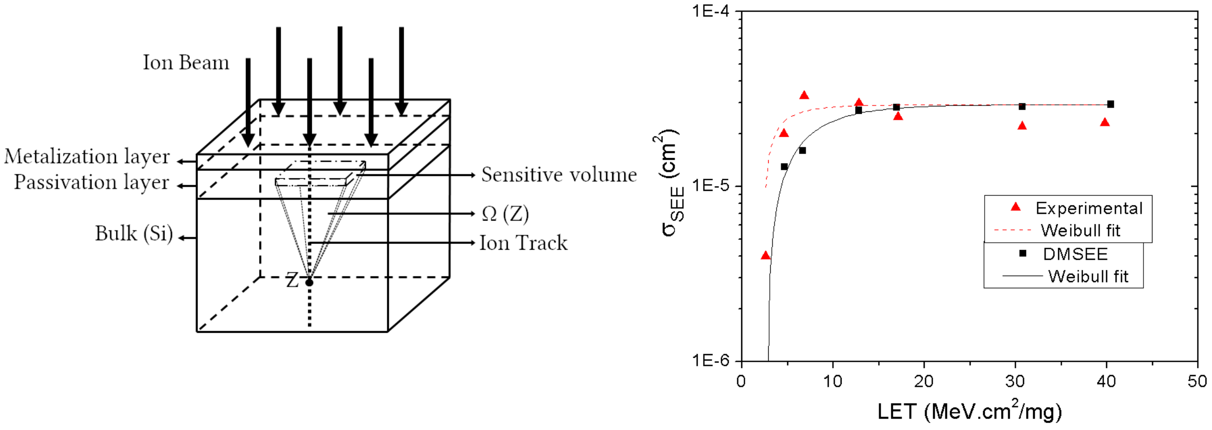

Figure 2. Geometry used for calculations and comparison between DMSEE and experimental results obtained in a pMOSFET (from [16]). The black solid line is a Weibull fit of the DMSEE data and the red dashed line is a Weibull fit of the experimental data.

4. Summary and Conclusions

In this work an experimental setup intended to study ionizing radiation effects in power MOSFETs and the basic framework of a Monte Carlo code for SEE cross section calculations in low-voltage MOSFETs, based on a diffusion model, were presented.

The test setup presented allows SET, SEGR and SEB measurements in MOSFETs. Although SEB is an entirely destructive effect, the proposed experimental setup allows SEB cross section measurements to be performed non-destructively due to the current limiting technique, reducing costs associated with destroyed DUT samples and lost facility test time. The main aspects for accurate SEE measurements in power transistors were presented and the considerations of circuitry were discussed in some detail.

DMSEE computational code was used for SEE cross section calculations in a low-voltage pMOSFET and the results obtained by computational simulation were compared to the experimental ones. Wrobel's diffusion method, used for SEU cross section calculations in SRAM memories, was successfully adapted to low-voltage MOSFETs, despite inherent differences related to the geometry, dimension sizes and critical energy of these devices.

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