Performance and Analysis of n-Type Vertically Stacked Nanowires Regarding Harmonic Distortion

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***Abstract*—This paper studies the harmonic distortion (or non-linearity) of vertically stacked SOI nanowires with different fin widths and channel lengths. The total harmonic distortion and third order harmonic distortion are used as figures of merit in this work. The harmonic distortion analysis is performed taking in consideration the differences between transistor's intrinsic voltage gain and transconductance over drain current ratio.**

Index Terms—stacked nanowires; harmonic distortion; MOSFET; SOI transistor

I. Introduction

The continuous advance of Integrated Circuits (IC) allowing an increased number of functions per chip, triggered the search for solutions that can provide both, improved gate control to overcome the short-channel effects as well as larger drain current without increasing the consumed silicon area [1]. One recent alternative being explored is the use of vertically stacked nanowires. It consists of multiple 3D stacked nanosheet levels of MOSFETs sharing the same gate, source and drain electrodes, behaving as one single transistor. Depending on the technology, the lower level has a trigate nanowire architecture and the levels above have a Gate-All-Around architecture [2].

Despite the continuous engagement in research of suitable components for digital applications, it's crucial that analog characteristics of newer devices are studied and optimized as well, since mixed analog-digital circuits comprise a far-reaching share of global electronic market. This fact is easily noticed by observing the amount of new products arriving and being consumed every day, which have a lot of functions that requires a decent digital/analog converter, such as mobile phones and computers with excellent cam recorders and sound speakers with better audio reproduction [3].

As the output characteristics of MOSFETs are very non-linear, when an input sinusoidal signal of a certain frequency is applied, the output signal will have the fundamental frequency and several high-order harmonics that are undesired. The amount of these undesired harmonics represents the harmonic distortion. The harmonic distortion (or non-linearity) is then amongst the analog figures of merit of a device.

The harmonic distortion is accounted by looking at the total harmonic distortion (THD), that refers to the overall amount of distortion added by the device, and the third order harmonic distortion (HD3), which is the first odd harmonic in the output signal.

To correlate specifically the non-linearity from MOSFETS and a day-to-day application, it is possible to stablish a relation between a component's total harmonic distortion and high-fidelity (hi-fi) audio streaming. As seen in [3], the total harmonic distortion of a class-AB amplifier, for example, is a common measure to indicate the sound reproduction quality of our media players. In addition, signal transmission on radio frequency circuits and applications require flawless performance of linearity on its electronic systems. Studies validating previously mentioned data can be found in [4].

This work aims to explore the harmonic distortion of two-level vertically stacked nanowires operating as single transistor amplifiers. Some of their basic electrical characteristics were presented in ref. [2]. However, to the best of our knowledge, the stacked nanowire harmonic distortion phenomenon has not been presented yet.

II. Characteristics of the Measured Devices

The devices used in this work are 3D stacked nanosheets with two levels made in Silicon-On-Insulator substrate: the lower level has triple gate SOI MOSFET architecture and the upper level is a Gate-All-Around (GAA) Si transistor. They were manufactured by CEA-LETI, with both Si channels of 9nm thickness (H_{FIN}). The gate stack is composed of a 2nm oxide (HfO_2) and a TiN and Tungsten metal [5].

Fig. 1 presents a TEM view of 2 stacked nanowires with different fin width (W_{FIN}) [5]. The total device channel width of stacked nanowire is a sum of widths from two levels of the device.

$$W_{(STACKED)} = W_{(TRIGATE)} + W_{(GAA)} = 4H_{FIN} + 3W_{FIN} \quad (1)$$

Regarding non-linearity analysis, n-type transistors with variable W_{FIN} of 10nm, 20nm, 40nm and a channel length of L=100nm, and a variable channel length of 100nm and 200nm with a constant W_{FIN} equal to 10nm were used.

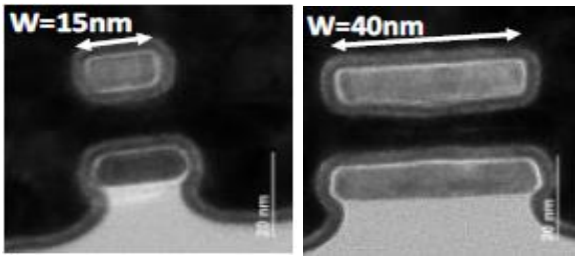

Fig.1 TEM image of stacked nanowires with different width [5]

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The extraction of harmonic distortion can be performed using AC measurements; however, these techniques are complex and require high demand on signal processing since they lead to a noisy output signal. The method itself adds non-linearities inherent of the extraction and signals of current are in µA magnitude [2].

On the other hand, the Integral Function Method (IFM) [6] allows the extraction of device's THD, HD3 and other distortion components using only DC curves of gate voltage and drain current. For devices operating as single transistor amplifiers, as in this work, the method assumes that an input sinusoidal signal with amplitude (V_A) is applied together with DC gate voltage and the linearity is accounted in the drain current.

III. Results

The measured drain current (I_{DS}) as function of gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$, V_{GS} being the gate voltage and V_{TH} the threshold voltage), extracted with a drain voltage (V_{DS}) of 750mV, are presented in Fig. 2. It is possible to see the increase of I_{DS} in larger W_{FIN} and smaller channel length transistors, as expected. The maximum values for V_{GT} were fixed on 0.33V to preserve transistors gate oxide integrity.

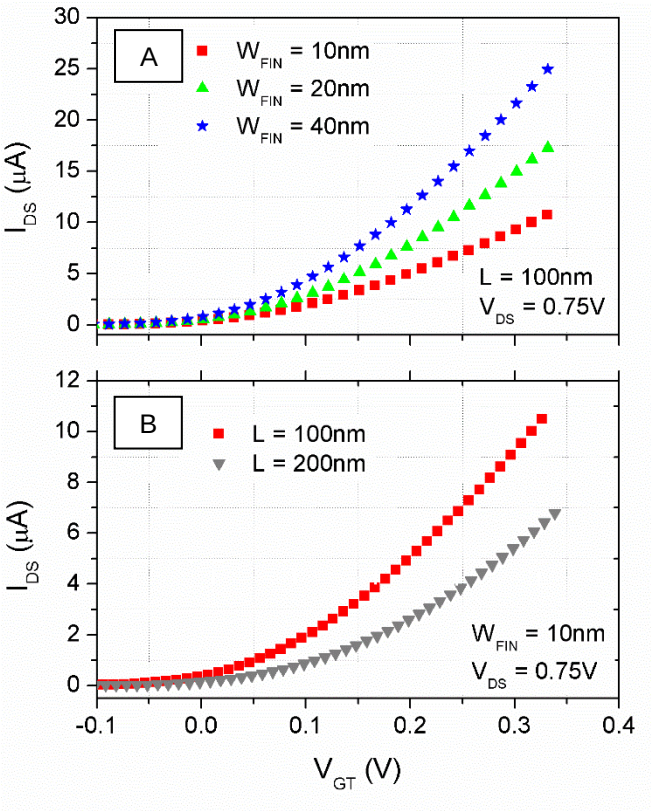

Fig.2 I_{DS} as function of V_{GT} curves, measured with V_{DS} = 0.75V, for stacked nanowires with (A) variable W_{FIN} (L=100 nm) and (B) variable L (W_{FIN}=10nm).

The IFM method has been applied on these data, considering a voltage amplitude (V_A) of 50mV. The figures of merit considered were THD and third order harmonic distortion (HD3), which shows if even or odds harmonics are preponderant in this transistor architecture. Fig. 3 presents the resulting THD and HD3 as a function of V_{GT} for all measured devices. Observing Fig. 3, one can see that the second order harmonic (HD2) is the major influencer of signal distortion for stacked nanowires: while THD varies between -20dB and -27dB, HD3 represents only a parcel between -50dB and -61dB.

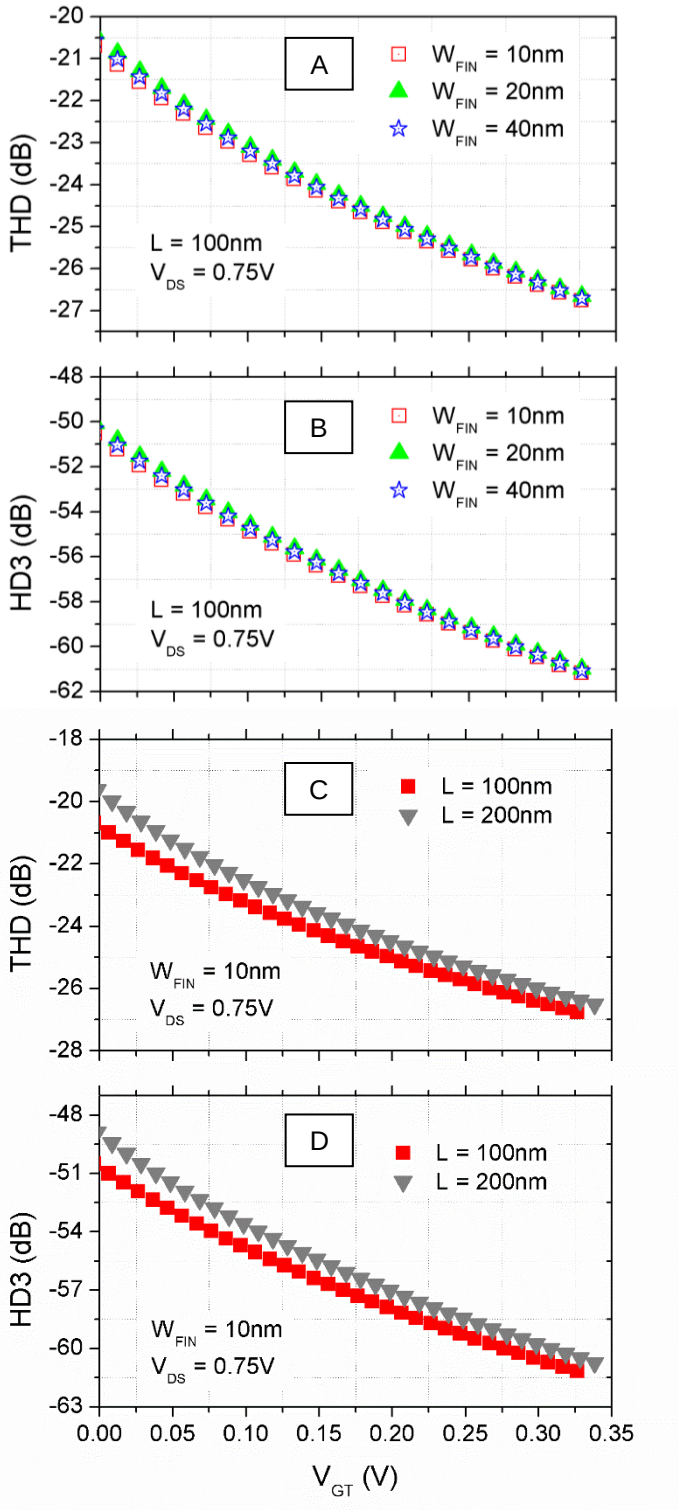

Fig.3 THD and HD3 as function of V_{GT} curves, extracted with V_{DS} = 0.75V and V_A=50 mV, for stacked nanowires with (A) - (B) variable W_{FIN} (L=100 nm), and (C) - (D) variable L (W_{FIN}=10nm), respectively.

Although it is possible to verify a slightly difference of non-linearity for L=100nm and L=200nm, W_{FIN} values did not show a major discretization with V_{GT} variation.

Despite this fact, it is important to state that all results are in agreement with theoretical equation of HD2 [7], which demonstrates inversely proportional relation between harmonic distortion with overdrive gate voltage.

$$HD2 = \frac{V_A}{V_{GT}\left[2+3(\theta+R_S K_{low})V_{GT}+(\theta+R_S K_{low})^2 V_{GT}^2\right]} \quad (2)$$

In eqn. (2), θ is the mobility degradation factor, R_S is the series resistance and K_{low} is the transistor gain described by eqn. (3), where μ_0 is the low field mobility and C_{OX} is the gate oxide capacitance per unit of area.

$$K_{low} = \frac{\mu_0}{1+\theta V_{GT}} C_{OX}\left(\frac{W_{(STACKED)}}{L}\right) \quad (3)$$

According to eqn. (2), for same V_{GT} and V_A, the dominating aspects determining HD2 are θ, R_S and K_{low}. For longer L and similar W_{FIN} there is a reduction in K_{low}, which is the responsible for the slight increase of HD2 seen for L=200nm with regards to L=100nm.

In order to get some insight on HD2 dependence on θ, R_S and K_{low}, the experimental I_{DS} *versus* V_{GS} curves measured at V_{DS}=25 mV were taken. The extraction of μ_0 and θ has been made using the method proposed in [8] whereas the R_S extraction has been made with the method proposed in [9]. Table I presents the obtained results for μ_0, θ and R_S for the devices with variable W_{FIN} and fixed L:

Table I. Extracted results of μ_0, θ and R_S for the measured stacked nanowires with variable W_{FIN} and fixed L, biased at V_{DS}=25 mV.

W_{FIN} (nm)	μ_0 (cm^2/Vs)	θ (V^{-1})	$R_S W$ (Ω*μm)
10	105.8	0.56	1391
20	101.4	0.35	1229
40	116.6	0.34	1413

The results presented in Table I indicate that the terms θ and $R_S.K_{low}$, which compose the denominator of eqn. (2), are of the same magnitude in the studied devices. This way, there is a balanced contribution of them in HD2 with no clear dominance of any.

As a result of low data discretization, another strategy was used: observation of distortions as function of g_m/I_{DS}. This propitiates an analysis with all devices biased on the same operational region, excluding V_{GT} dependency.

These new comparisons are found in Figs. 4 and 5, that present the THD and HD3 of measured devices as a function of g_m/I_{DS} for fixed L and W_{FIN}, respectively. Once again values are close together with each other, but it is possible to establish somewhat resemblance with THD and the different W_{FIN} of transistors: W_{FIN} = 40nm has the largest non-linearity amongst other devices. All of them present a lower distortion with reduction of g_m/I_{DS}, in accordance with previously results found in Fig. 3 and eqn. (2), since the V_{GT} increase leads to smaller g_m/I_{DS} values.

For the devices with variable L biased at the same g_m/I_{DS}, one can see that THD and HD3 are weakly dependent on L. in the studied bias range.

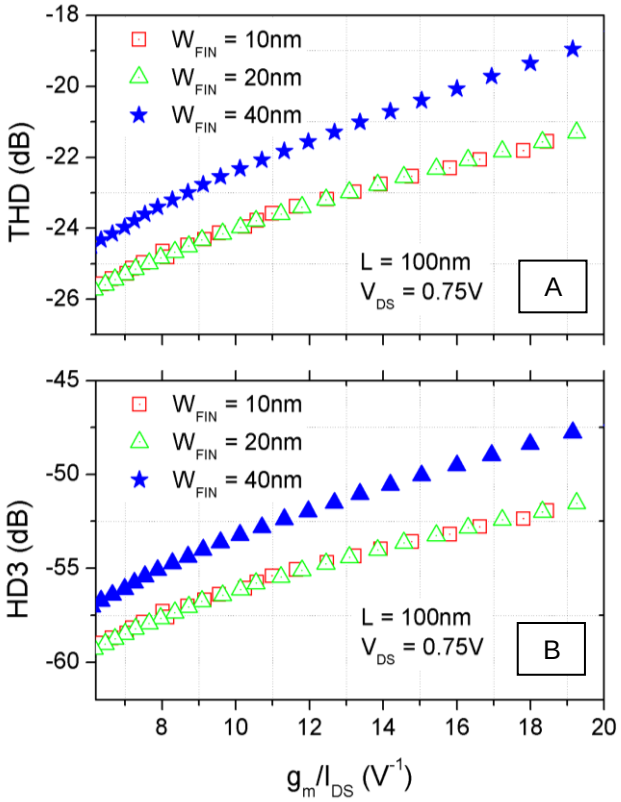

Fig.4 Extracted (A) THD and (B) HD3 as function of g_m/I_{DS} curves for stacked nanowires with variable W_{FIN} (L=100 nm) at V_{DS}=0.75V and V_A=50 mV.

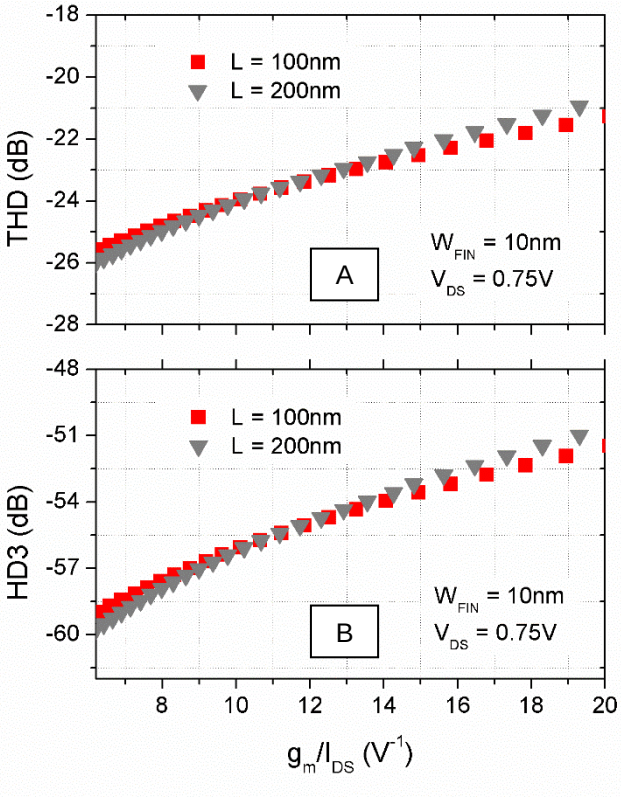

Fig.5 Extracted (A) THD and (B) HD3 as function of g_m/I_{DS} curves for stacked nanowires with variable L (W_{FIN}=10 nm) at V_{DS}=0.75V and V_A=50 mV.

From Fig. 5 it is possible to see that for the devices with variable L biased at the same g_m/I_{DS}, THD and HD3 are weakly dependent on L in the studied bias range.

An even better perspective can be achieved by using intrinsic gain voltage (A_V) extracted in [2]. Tables II and III associate different widths and lengths with their respective values for V_{GT}, g_m/I_{DS} and A_V.

Table II. Correlation between V_{GT}, g_m/I_{DS} and A_V for the stacked nanowires with variable W_{FIN} and L=100 nm.

W_{FIN} (nm)	V_{GT} (mV)	g_m/I_{DS} (V^{-1})	A_V (dB)
10	100	12.04	41.34
	200	7.53	37.83
	300	5.00	32.33
20	100	13.02	41.09
	200	7.91	37.94
	300	5.17	32.67
40	100	12.70	38.08
	200	8.06	35.83
	300	5.12	32.09

Table III. Correlation between V_{GT}, g_m/I_{DS} and A_V for the stacked nanowires with W_{FIN}=10nm and variable L.

L (nm)	V_{GT} (mV)	g_m/I_{DS} (V^{-1})	A_V (dB)
100	100	12.04	41.34
	200	7.53	37.83
	300	5.00	32.33
200	100	13.68	53.55
	200	8.79	42.60
	300	6.21	34.75

All devices show similar comportment, decreasing the gain with higher gate voltage overdrive. Such tendency is expected considering that in this voltage range the stacked nanowires are moving towards moderate to strong inversion region, exhibiting a decrease in A_V as previously reported in [10]. As the devices have different A_V, the amplitude of the output signal with similar input signal amplitude will be different, which could be pointed as the cause of the larger distortion amongst them.

To decorrelate the different A_V and the distortion data, Fig. 6 presents the THD/A_V and HD3/A_V as function of g_m/I_{DS} for devices with constant L and W_{FIN}.

The direction of the curves has changed as a result of the lower A_V values as g_m/I_{DS} reduces. Besides, the main contribution for new plots is the completely separated points, facilitating the analysis.

Finally, one last comparation can be made to get insight on the reasons for the different THD. It is known that the HD2 can be obtained by the derivative of the transconductance, as indicated in eqn. (4) [11]:

$$HD2 = \frac{V_A}{4}\frac{\frac{\delta g_m}{\delta V_{GT}}}{g_m} \quad (4)$$

Fig. 7 presents the calculated dg_m/dV_{GT} as a function of g_m/I_{DS} for the experimental devices with variable W_{FIN}, biased with V_{DS}=0.75V and V_A=50 mV.

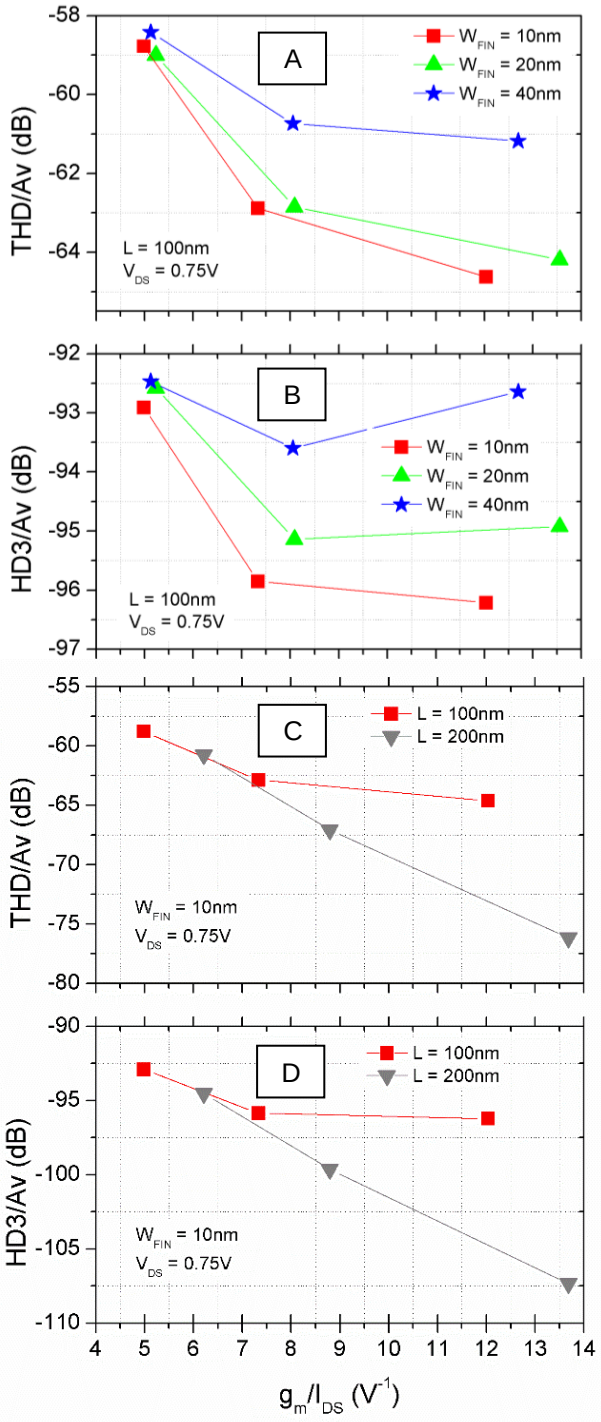

Fig.6 THD/A_V and HD3/A_V as function of g_m/I_{DS} curves extracted with V_{DS} = 0.75V and V_A=50 mV, for stacked nanowires with (A) - (B) variable W_{FIN} (L=100 nm), and (C) - (D) variable L (W_{FIN}=10nm), respectively.

By plotting dg_m/dV_{GT} as function of g_m/I_{DS} it is possible to see that W_{FIN} = 40nm, which has larger fin width among the devices, has the greatest variation and is also the one with higher THD, aligned with Fig. 4, eqn. (4).

The results presented in this work can be compared with those from [12], which studies single level nanowires with variable W_{FIN} and similar gate stack, although the channel length and V_{DS} are different. The fin width dependence is similar, showing that wider devices presented worst linearity than narrower ones because of the larger dg_m/dV_{GT}.

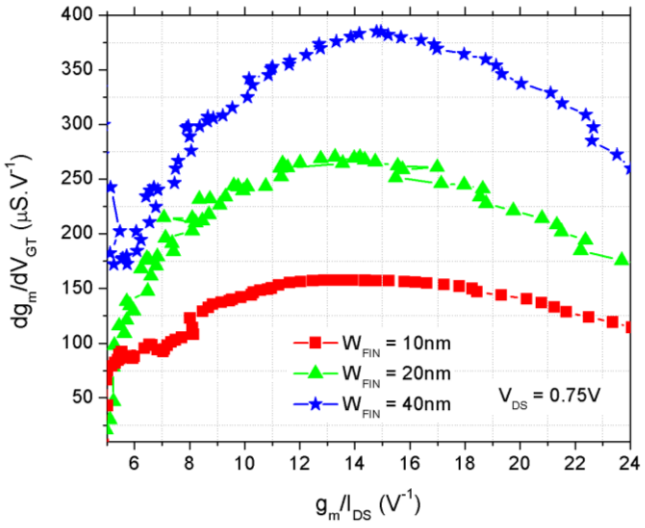

Fig.7 Calculated dg_m/dV_{GT} as function of g_m/I_{DS} curves for the stacked nanowire transistors with L=100 nm and variable $W_{FIN,}$ biased with V_{DS} = 0.75V and V_A=50 mV.

Regarding THD and HD3, one can notice that for V_{GT}= 300mV, both stacked and single level nanowires present THD around -26.5 dB. Observing THD *versus* g_m/I_{DS} equal to 12 V^{-1}, the non-linearity of vertically stacked nanowire varies between -23.5 dB and -22 dB (Fig. 4). On the other hand, for the single level nanowire transistor, this value is around -25 dB for W_{FIN}=9.5 nm.

IV. Conclusions

This paper presented the harmonic distortion of 2-level stacked nanowires with variable fin width and channel length. For all studied transistors, the harmonic distortion is dominated by the second order harmonic distortion, with 30 dB larger than the third order harmonic distortion. After decorrelating the harmonic distortion from the device intrinsic voltage gain, it has been demonstrated that devices with wide fin width presented larger harmonic distortion than narrow ones, in all operational regions. It is caused by the larger variation of the transconductance with the gate voltage overdrive. Also, longer devices present greater harmonic distortion than short ones.

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