Substrate Effect Evaluation by the Analysis of Intrinsic Capacitances in SOI UTBB Transistors

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***Abstract*— The main goal of this paper is to present the behavior of the substrate effect in Ultra-Thin Body and Buried Oxide (UTBB) SOI MOSFETs with respect to the back gate bias (V_{sub}) through DC and AC simulations validated to experimental data from the literature. Different ground plane (GP) arrangements have been considered in order to enhance the analysis. It has been shown that the substrate effect is strongly influenced by the reduction of the back gate bias. The P-type GP devices has shown lower capacitances and the capacitive coupling of the structure presents a different behavior with respect of each kind of GP configuration as the back gate bias is varied. Finally, it has been shown that the GP below the source and drain regions contributes significantly to the overall capacitive coupling of the transistors.**

***Index Terms*— UTBB; Substrate Effect; Body Factor.**

I. INTRODUCTION

From the middle of 60´s until nowadays, the crescent demand for processing and velocity with low power consumption has led the semiconductor industry to a strong development, which can only be achieved by the increase of the integration levels. To reach the ultra large scale of integration (ULSI), the reduction of the devices dimensions has tried to follow the Moore´s Law [1]. The miniaturization of MOS devices came up with the undesirable influence of the source and drain junctions depletion regions on the channel charges, degrading their output characteristics. These effects are so-called Short Channel Effects (SCEs) [2].

To minimize the influence of SCEs, new technologies were developed, being the Silicon-on-Insulator (SOI) one of the most promising [3]. This technology is based on the introduction of a layer of insulating material, usually composed by SiO_2, called buried oxide (BOX) that separates the active region of the chip, where the devices are fabricated, from the substrate of the silicon wafer, leading to a better capacitive coupling of the structure. Due to the worse thermal conductivity of the SiO_2 in relation to the silicon, SOI devices suffer from an undesirable effect called self-heating effect (SHE) [4].

The heat dissipation, which has its main path by the silicon of the substrate is impaired, causing a temperature increase in the channel region and reducing the carriers' mobility. This effect leads to a degradation in the output characteristics, which can culminate with a negative output conductance [5].

Along the last years, several improvements have been proposed to SOI devices and one of them constitutes in the thinning of the active silicon layer, leading to the development of Ultra-Thin Body MOSFETs (UTB) [6], which presents an active silicon layer thickness (t_{si}) in the order of 6-10 nm. However, due to the smaller silicon area in the active region, this technology has the penalty of degrading the thermal conductivity of the devices, increasing the influence of the SHE in the I–V output characteristics [7].

As an evolution of the UTB technology, a new arrangement of SOI device, the Ultra-Thin Body and Buried Oxide (UTBB) SOI MOSFET, presenting both silicon and buried oxide in ultrathin layers, was developed. In such device, the BOX thickness (t_{box}) is in the order of 10-25 nm [8] while the silicon layer one is kept in the order of 6-10 nm. The reduced t_{box} in UTBB transistors opens the possibility of the active substrate biasing, making it works as a second gate, also known as back gate, which can efficiently be used to improve the performance of the device when it operates in analog and RF applications [9]. The implementation of a high doped thin layer of silicon below the BOX, called Ground-Plane (GP) [9], allows for the back biasing of single devices and contributes to reduce the depletion in the substrate region. The reduced BOX thickness contributes to a better heat dissipation, making UTBB devices less susceptible to the SHE. On the other hand, the insulating becomes less efficient in UTBB devices, causing an undesirable coupling of the substrate with the source and drain regions, so-called substrate effect (SUB) [10], which also degrades the devices output characteristics.

Such degradation can be evaluated through the Body Factor of the devices (α), that indicates the dependence of the threshold voltage with the substrate bias and which may be affected by the parasitic coupling between the substrate and the source and drain regions. For that reason, the present work aims at evaluating how the back biasing and the different set of GP arrangements affect the capacitive coupling of the structure. The entire work has been performed through numerical 2D AC and DC simulations of the I-V and C-V curves of the devices, validated to experimental data from the literature.

II. DEVICES CHARACTERISTICS

The simulated structures present channel doping concentration of $1x10^{15}$ cm^{-3}, gate oxide thickness (t_{ox}) of 2 nm, active layer thickness (t_{si}) of 7 nm, gate length (L) of 100 and 25 nm, and buried oxide thickness (t_{box}) of 10 and 25 nm. The source and drain regions are doped with arsenic with a concentration of $5x10^{20}$ cm^{-3} with elevated source/drain extensions of 15 nm. The GP thickness has been considered equal to 10 nm with $1x10^{18}$ cm^{-3} constant doping concentration of arsenic (As) for the n-type GP and boron (B) for the p-type GP. The work was developed through DC

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and AC simulations at Synopsys Sentaurus TCAD [11]. Models accounting for the carrier's generation and recombination, bandgap narrowing, mobility dependence on vertical and longitudinal electric fields and quantum effects have been considered in all the simulations running under the hydrodynamic transport mechanism.

As mentioned before, UTBB devices suffers with undesirable effects from the substrate coupling (SUB) and the Self-Heating (SHE), which promotes a degradation of the output conductance (g_D) at low frequency and, under a strong influence of these effects, g_D can reach negative values [12-14]. Both SUB and SHE effects can be evaluated by a technique called AC conductance [12], this technique constitutes of the application of a small signal in a wide frequency range to the gate terminal followed by the observation of the signal response with respect to the applied frequency. Fig. 1 presents the behavior of g_D, extracted as a function of the frequency and the degradations due to self-heating and substrate effects can be seen. As one can observe, there are three distinct regions along the curve, indicating that g_D is not constant along the frequency spectrum. The first g_D transition is related to the substrate effect where the minority carriers in the substrate do not respond to the AC signal ($\Delta g_{DSUBMIN}$). The second transition is related to the removal of the dynamic SHE (Δg_{DSH}) and the third one is related to the substrate effect where the majority carriers ($\Delta g_{DSUBMAJ}$) in the substrate do not respond to the applied AC signal [10,15,16]. It is worth mentioning that, below 3 MHz, one can observe negative values for g_D, indicating an intense influence of the SHE and SUB.

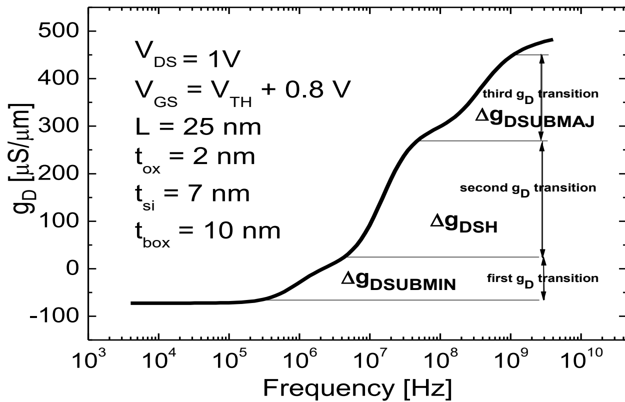

Fig.1. Output conductance (g_D) as a function of the frequency for UTBB device with L = 25nm and t_{box}= 10nm, indicating the g_D transitions due to self-heating (Δg_{DSH}) and substrate effects due to minority and majority carriers ($\Delta g_{D\ SUBMIN}$ and $\Delta g_{D\ SUBMAJ}$, respectively)[16].

Fig. 2 presents the curves of g_D as a function of the frequency for devices with t_{box} equal to 10 and 25 nm and, as one can observe, the device with a thicker BOX present a reduced $\Delta g_{DSUBMIN}$. Although not so apparent as $\Delta g_{DSUBMIN}$ difference for devices with t_{box} = 10 and 25 nm, Δg_{DSH} increases with t_{box}. For t_{box} = 25 nm, Δg_{DSH} = 34 μS/μm against 29 μS/μm in the thinner BOX. As the focus of this work is on the substrate effect, the overall analysis will be performed in devices with thinner BOX.

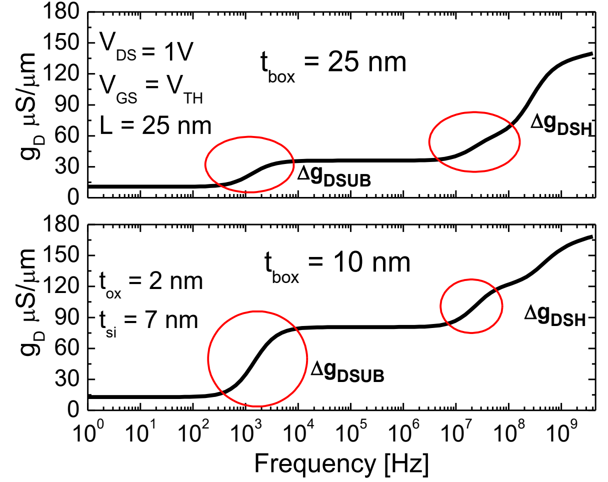

Fig.2. Output conductance (g_D) as a function of the frequency for UTBB device with L = 25nm and t_{box}= 10 and 25nm.

To validate the simulated results, the simulations were initially performed for devices with physical characteristics identical to the ones from [15] with the channel length equal to 100 nm and (t_{box}) of 10 and 25 nm in order to obtain electrical and thermal behaviors close to the ones obtained in the experimental device as performed in [16]. The contacts of gate, source, drain and substrate represent the points in a simulated device that interact with the ambient in terms of heat dissipation and thermal energy transfer. To achieve results near to the experimental work, the thermal resistivity of the source, drain and substrate electrodes were set as 0.00035 cm^2K/W for source and drain and 0.00017 cm^2K/W for the substrate. The gate terminal has been considered adiabatic since the passivation layer above the gate is too thick for heat removal through the gate stack [17]. The thermal resistivity at the substrate is smaller since the substrate is the main heat path for any device. The results of the simulated work against the experimental ones are shown in Table I.

It is shown an increase in the thermal resistance with a BOX increase from 10 to 25 nm. All the simulation data have shown errors smaller than 5% with respect to the experimental results, validating the simulations.

Table I. *Comparison between the simulated data and the extracted parameters presented by experimental devices as performed in [16].*

Parameter	t_{box}	Data Comparison		
		Simulation	*Experimental*	*% Error*
Drain Current [mA/μm] (@V_{GS} = V_{TH} + 0.8 V and V_{DS} = 1 V)	10 nm	0.55	0.55	0
	25 nm	0.80	0.80	0
Thermal Resistance (R_{TH}) [μm K/mW]	10 nm	69	70	1.42
	25 nm	80	84	4.34

III. Body Factor Analysis

Initially, simulations were performed to verify the impact of the back bias considering UTBB structures with p-type GP (B Full), n-type GP (As Full) and without GP (No Gp) [9]. The most common GP used for nMOS devices consists in a p-type, doped with boron (B), which can be reached through proper V_{sub} biasing, enabling multi-V_{TH} devices as well as

improved capacitive coupling. In order to verify the effect of the source and drain regions on the substrate effect as mentioned in [10], simulations were performed for two different GP configurations, one considering GP only below the channel region (CH Gp) [18] and other with the GP only below the source/drain regions (S/D Gp) [19]. All the GP configurations are shown in Fig.3.

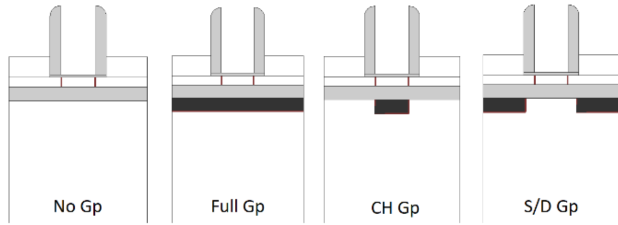

Fig.3. *Devices presenting the different GP arrangements (in black) used in this work.*

The threshold voltage (V_{TH}) was extracted as a function of the back gate bias (V_{sub}) using the technique exposed in [20] for each different kind of GP to verify how V_{TH} behaves with respect to the different GP arrangements. Fig. 4 (A) presents the results of the Full Gp devices, Fig. 4 (B) the results of the CH Gp ones and Fig. 4 (C) the data of the S/D Gp, all of them with the curve related to the No Gp device as a reference.

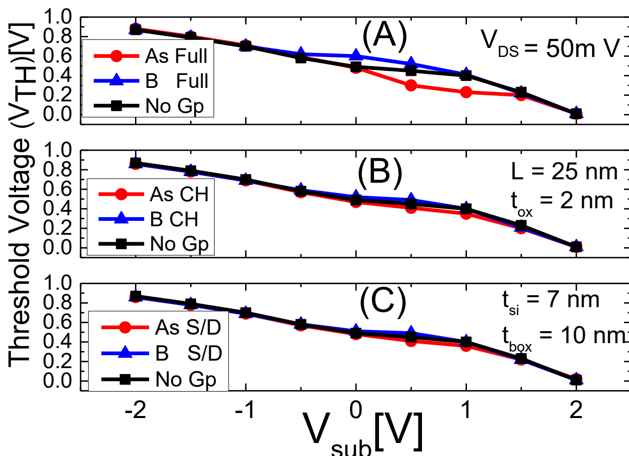

Fig.4. *V_{TH} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

One can observe an increase of V_{TH} with the decrease of V_{sub} for all the structures, which occurs due to the reduction of the surface potential on the second interface between the silicon of the channel and the BOX. A detailed analysis of such effect is performed in [21]. It can be observed that a different behavior is obtained in Fig. 4 (A) for V_{sub} between -0.5 and 1 V. In this interval one can observe a behavior like the one presented in [22] and this result can be correlated to the variation of the potential on the second interface and to the different workfunctions of each kind of GP layer. When the GP layer does not cover the whole device, this effect is reduced.

The body factor is denominated as the relation between the threshold voltage (V_{TH}) and the substrate bias, ($\alpha = \Delta V_{th} / \Delta V_{sub}$) and, in this work, it was obtained through the equation (1) described in [21] for UTBB devices.

$$\alpha = \frac{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}(X_{bar})}{t_{box} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}(t_{si} - X_{bar})} \quad (1)$$

where t_{ox} is the gate oxide thickness, t_{box} is the buried oxide (BOX) thickness, ε_{ox} is the permittivity of the silicon dioxide, ε_{si} is the permittivity of the silicon, t_{si} is the thickness of the silicon layer in the channel and X_{bar} represents the point of the silicon layer between top and buried oxide in which the centroid of charge Q_{si} is located, i.e. the vertical position in the channel where there is the highest concentration of electrons. This point can be seen in Fig. 5, which represents the electron concentration along the silicon thickness. It was obtained through a vertical cut in the center of the simulated structure. One can observe that, for V_{sub} equal to -2 V, the centroid is close to the gate oxide/channel silicon interface. For V_{sub} equal to 0V, the centroid is in the center of the channel and, for V_{sub} equal to 2V, the centroid is close to the channel silicon/BOX interface. X_{bar} is the distance between the gate oxide/channel silicon interface and the centroid.

Fig. 6 (A), (B) and (C) present the behavior of the body factor calculated through (1) as a function of V_{sub} for the different GP arrangements. For V_{sub} from -2 to -1 V and in the interval between 1 V and 2 V, the body factor does not present substantial change between the different GP arrangements. However, for V_{sub} from -0.5 to 1 V, there is a notable difference between the kinds of GP. For the configuration with n-type GP, the flat-band voltage of the BOX interface (V_{fb2}) is about -0.76 V whereas for p-type GP, V_{fb2} = 0.18 V. For the structure without GP, V_{fb2} = 0 V. For that reason, the interface between channel and BOX in devices with n-type GP starts to deplete for lower V_{sub}, causing the differences observed in Fig. 4.

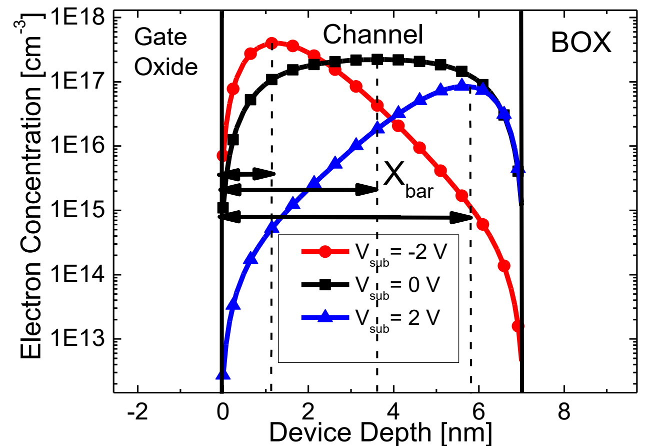

Fig.5. *Electron concentration along the device depth in the center of the structure for a 25 nm-long device without GP biased with $V_{GS}=V_{th}$, V_{DS}=50mV for different V_{sub}.*

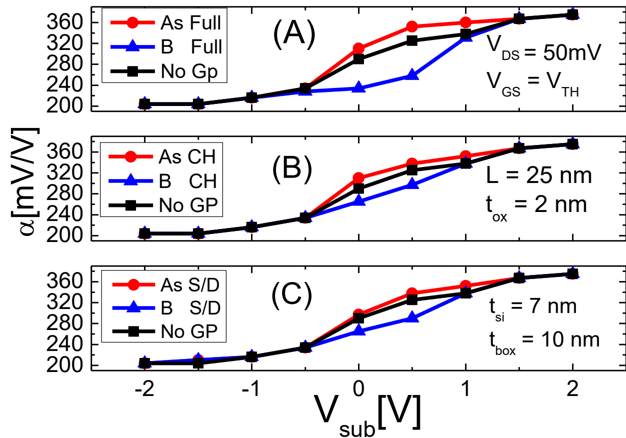

Fig.6. *The Body Factor as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

From Figs. 6 (B) and (C), it can be observed that not only the presence of the GP below the channel, but also below the source/drain regions contribute for the behavior of the structure with Full GP, indicating that the spreading electric field induced by the GP under the source/drain regions also affects the charges centroid in the channel. Finally, for $V_{sub} \leq -1$ V and $V_{sub} \geq 1$ V, where all the curves are similar, a variation of α is also observed, indicating the supercoupling of the structure as described in [23].

IV. Capacitive Coupling Analysis

In order to deep evaluate the behavior of the particular interval of V_{sub} where the body factor is influenced by the GP type, AC simulations were performed, and the intrinsic capacitances were extracted with the application of a signal with the frequency of 10 kHz to the gate terminal of the devices.

This analysis has taken into account only the intrinsic capacitances affected by the substrate biasing. In this context, Figs. 7 to 10 present the capacitances C_{bb}, C_{gb}, C_{sb}, C_{db} and, respectively, which correlate the charge variation at the substrate, gate, source and drain electrodes to the back-bias variation. Initially, the capacitances have been extracted for low drain bias (V_{DS} = 50 mV) to avoid the drain potential influence in the analysis.

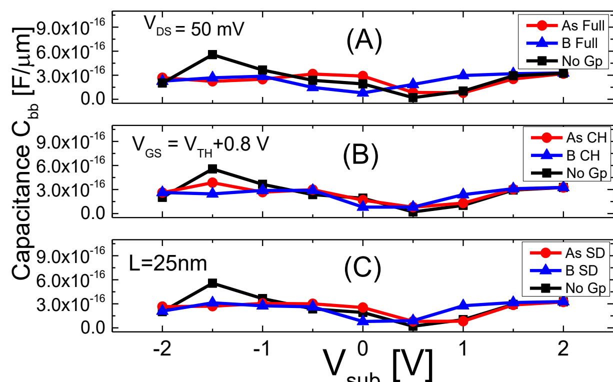

Fig.7. *The substrate capacitance C_{bb} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

In Fig. 7, it can be observed that the C_{bb} capacitance remains in the order of 1-6 x 10^{-16} F/µm. This capacitance is given mainly by the buried oxide capacitance, which can be calculated as $(\varepsilon_{ox}/t_{box}).(L+L_{SD})$, being L_{SD} the source/drain lengths (equal to 30 nm), and results in 2.93x10^{-16} F/µm for the transistors with L = 25 nm and t_{box} = 10 nm.

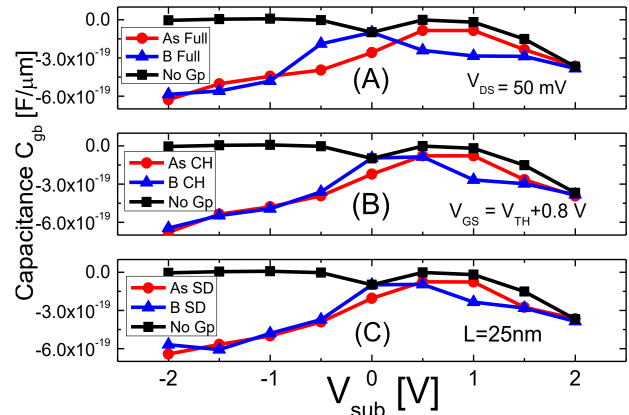

Fig.8. *The gate capacitance C_{gb} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

As it could be expected, the gate-to-substrate capacitances shown in Fig. 8 are significantly smaller than the ones obtained for C_{bb} in Fig. 7 since the variation in the gate charges is not expected to be affected by the substrate potential shift.

In Figs. 9 and 10, it is shown that the source-to-substrate and drain-to-substrate are several orders of magnitude larger than C_{bb} and C_{gb}, indicating that the former ones are responsible for the substrate effect presented by the devices. For that reason, from now on, the overall analysis will be focused on C_{sb} and C_{db}. One important characteristic of such capacitances is related to their symmetry to each other. For $V_{sub} \geq 0.5$ V, both C_{sb} and C_{db} tend to the order of magnitude of the buried oxide capacitance. Apparently, for such V_{sub}, the variation in the substrate bias induces a change in the amount of charges of the entire channel. However, for $V_{sub} < 1$ V, C_{sb} and C_{db} exhibit similar absolute values, being C_{sb} positive and C_{db} negative. In this case, it seems that an alteration in V_{sub} affects differently the channel charge close to the source and drain regions, i.e. the charge is reduced in one of the sides and increased in the other.

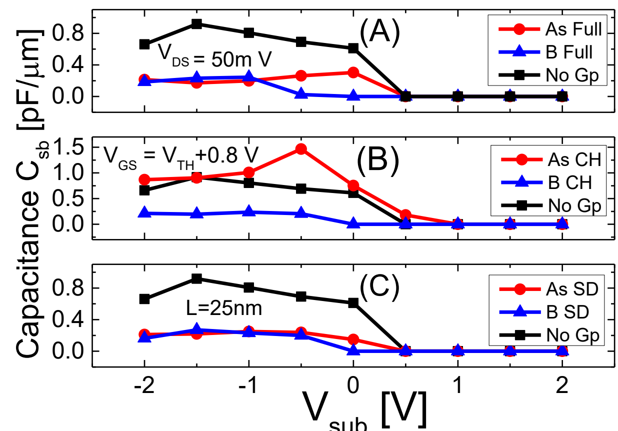

Fig.9. *The source capacitance C_{sb} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

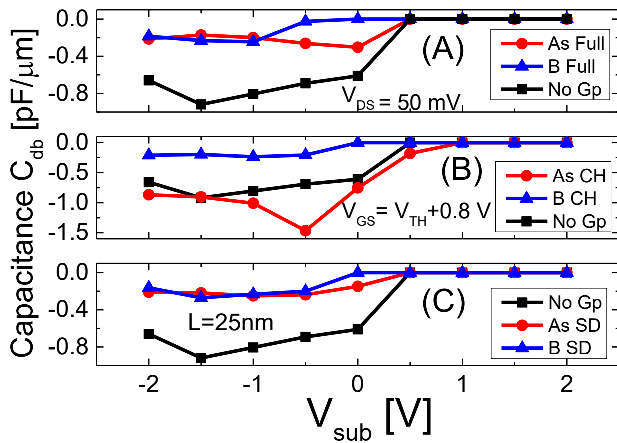

***Fig.10**. The drain capacitance C_{db} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

The shapes of the C_{sb} and C_{db} curves as a function of V_{sub} explains the variation of the body factor with the substrate bias shown in Fig. 6. For lower values of V_{sub}, there is an increase in the source and drain capacitances, improving the capacitive coupling of the structure. On the other hand, for larger V_{sub}, C_{bb} prevails over the other capacitances, degrading α.

The effect of the drain voltage in the capacitances is shown in Fig. 11, which present C_{sb} extracted with the device operating in saturation, with V_{DS} = 1 V. In Fig. 11(A), it can be observed the global effect of the GP on the behavior of the curves. In this case, it can be observed that, for n-type GP (As Full), the absolute capacitance values are larger in the interval between $-1 \leq V_{sub} \leq 1$ V, which indicates a stronger effect of the substrate in the charges at source/drain electrodes and that p-type GP transistor presents lower parasitic capacitances than the other configurations. Fig. 11 (B) and (C) also corroborate to demonstrate that the spreading field due to GP below source/drain plays an important role in the overall capacitive coupling. For back gate bias ≤ -1 V, there are no significantly changes in the capacitance values for the different kinds of GP, indicating the supercoupling phenomenon when the devices are biased in this range of back gate values. For back gate bias > 1 V, the presence of the supercoupling can also be seen, indicating that for high values of back gate than this point, the phenomenon prevails, and there are no more changes in the capacitance values. When comparing the curves for V_{DS} = 1 V to the ones obtained for V_{DS} = 50 mV, it is possible to note that the main difference is related to the absolute values obtained for C_{sb} at lower V_{sub}, which can be related to the increase in the unbalance of the charges closer to the source and drain of the device.

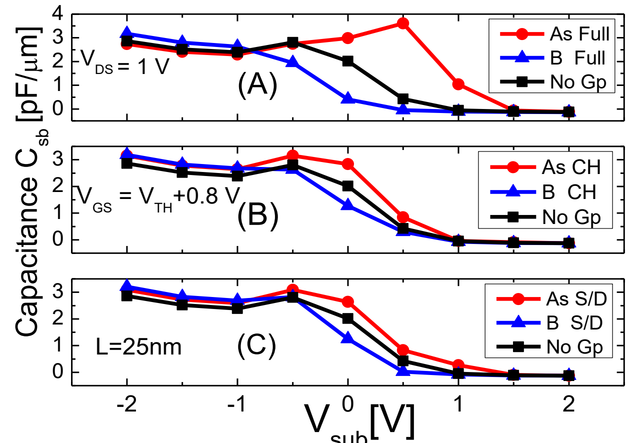

***Fig.11**. The source capacitance C_{sb} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

To evaluate the effect of the channel length, the same capacitance analysis was performed for a 100 nm-channel length device. In Fig. 12, one can observe the capacitances in a device operating in saturation regime, at V_{DS} = 1 V. As the capacitance can be defined as a charge variation due to voltage application [24] and, in both channel lengths, the drain and the source capacitances present the same amplitude with an opposite value, it indicates the same influence of the substrate coupling with the source and drain regions at the same amplitude, but with opposite charge variation similarly as observed in the shorter device.

In relation to a 25 nm device, the source capacitances in Fig. 12 present higher values indicating a more accentuated effect of the substrate with the source and drain regions, which is related to the larger channel area of the structure. By comparing the curves of 25 nm and 100 nm-long devices for different GP configuration, it is also possible to evaluate the spreading capacitances in the devices. In Fig. 11 (B) and (C) (for 25 nm-long devices), the curves shown for each GP configuration are similar, whereas in Figs. 12 (for 100 nm-long devices), the capacitance values, considering the GP only below the channel (figure (B)) are higher than the ones observed for GP below source and drain (figure (C)). This effect is more clearly seen for the Arsenic GP and related to the lower influence of the spreading capacitance in longer devices.

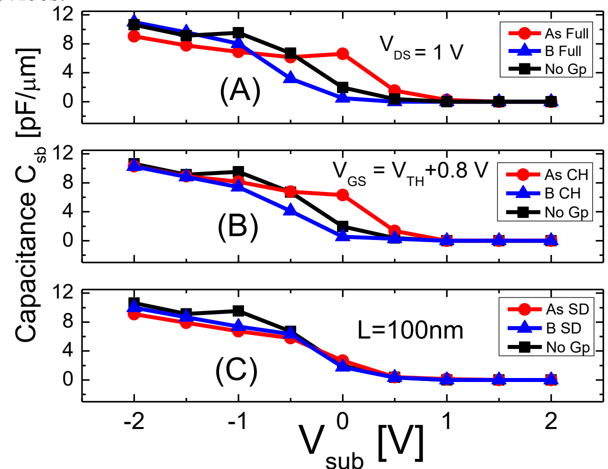

***Fig.12**. The source capacitance C_{sb} as a function of V_{sub} for devices without and with Full Gp in (A), for devices without and with CH Gp in (B) and for devices without and with S/D Gp in (C).*

V. CONCLUSIONS

This work has evaluated how the body factor through the different capacitive couplings provided by the different type of GP arrangements is affected by the substrate effect in SOI UTBB transistors. It was demonstrated that the different flat-band voltages of the channel/BOX interface influence the charge centroid position in the channel, as the back gate bias is varied. This effect is responsible for altering the threshold voltage of the devices due to the different capacitive couplings obtained. The results of this work from the perspective of parasitic coupling indicates that p-type GP transistor presents lower parasitic capacitances than the other configurations. Such reduction is observed mainly at lower substrate biases, corroborating with different studies from literature than point out such conditions as best ones for analog operation. In the back gate interval for which the body effect is different between the devices, the p-type GP has shown a lower capacitance, indicating a reduced substrate effect. The same effects were observed in device with a 100 nm channel length except for presenting higher absolute capacitance values. For back gate bias lower than -1 V and larger than 1 V the devices do not present significative changes in the capacitive couplings for different GP configurations. In this case, the supercoupling of the structure prevails in this interval of back gate biases.

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