

Effect of Interface Traps on the RTS Noise Behavior of Junctionless Nanowires

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Abstract— This work presents a study on the effects of interface traps throughout the Junctionless Nanowire Transistor (JNT). The results are obtained by analyzing the Random Telegraph Signal noise of the device against frequency, which consists of an exception of the generation-recombination noise. The results obtained are mostly from numerical simulations, validated through experimental data. It has been considered a decrescent exponential trap profile along the bandgap. The traps are distributed from the conduction band to the valence band. It was possible to verify that the RTS of junctionless devices presents two different well-defined behaviors when biased at different operating regimes. At partial depletion, a noise plateau has been observed with small variation in the corner frequency, indicating a small variation of the carriers' lifetime. At accumulation, the noise plateau reduces with the gate voltage and the corner frequency increases, indicating a reduction in the carriers' lifetime.

Index Terms—Junctionless; Nanowire; Low-Frequency Noise; Random Telegraphic Signal (RTS).

I. INTRODUCTION

Understanding the noise behavior of new devices is essential for implementing them in commercial applications. Without knowing correct data on this topic, a project is very likely to fail, since the sum of noise-related effects can generate unexpected results at the signal the circuit is processing. In this work, it is considered as noise, random perturbations that are inherent to the physics of the device [1]. External noise sources such as vibrations and adjacent circuits are not considered in this work.

The device which is the topic of this study is the Junctionless Nanowire Transistor (JNT) [2]. The main advantage of a JNT is the constant doping from drain to source, such that there are no abrupt junctions and no doping gradients. Factors such as the formation of abrupt junctions are very difficult to implement on devices with channel length under 20nm, making the JNT a very promising device for small technological nodes. To improve the electrostatic control of the gate, another technology known as multi-gate, which consists on the creation of gate connections all around the device channel, has been applied. There are different kinds of implementation for this technology. The JNTs are usually implemented in triple gate.

The main goal of this work is to obtain the behavior of the JNT for a specific kind of low frequency noise, the Random Telegraph Signal (RTS) noise. Such signal is usually evaluated along time, but it can also be analyzed in the frequency [1]. The RTS is considered a special case of the generation-recombination noise. Considering a single or a small sample of traps with similar characteristics such as Energy

level, capture and emission times, one can obtain a disturbance at the signal that is represented by an oscillation between two discrete levels. The capture and emission processes change the electrical charge within the oxide-silicon interface and, therefore, the surface potential suffer a fluctuation. The trapped charges can also impact the carrier mobility, diffusion coefficient, electric field, barrier height and space charge region width [1].

In this device, there are two current components. The first occurs within a neutral area near the center of the device. This conduction path is present for gate voltages (V_{GS}) above threshold (V_{TH}) and lower than the flatband voltage (V_{FB}). In this condition the device is partially depleted, which results in a surface potential farer from the conduction band edge, i.e. a lower potential is observed at surface with respect to the center of the device. As the traps usually present activation energy closer to the conduction band, the probability of occurring capture/emission events is low, i.e. traps are mostly in a steady-state regime either occupied or vacant, once there is no energy for them to be capturing or emitting carriers. So, the effects of the RTS noise are less significant. As the gate voltage increases in the direction of V_{FB} , the neutral path becomes larger and conduction occurs closer to the gate dielectric-silicon interface. Thus, the traps start emitting and capturing carriers, resulting in significant fluctuations on the drain current (I_D).

When $V_{GS} > V_{FB}$, another conduction mechanism is enabled: the accumulation layer conduction. Next to the oxide-silicon interface, the device starts to accumulate carriers, making the carriers' density (n) in this region higher. This increase on n changes the local Fermi level and the traps profile that are more susceptible to trapping and emissions. Since fundamental characteristics of the device suffer fluctuation, a series of consequences may happen, such as fluctuation on the threshold voltage (V_{TH}).

Considering the working mechanism of the JNT and its sensibility to this specific kind of noise, this work was proposed, focusing on how few traps with similar characteristics may affect the noise of the device and, consequently, its operation. Most papers presented in current literature about low frequency noise in Junctionless transistors [3-6] perform a qualitative noise analysis without correlating the obtained curves to the traps' characteristics, such as its cross section and activation energy. So that, the main goal of this work is to provide more information on the low frequency noise behavior of the JNT considering the RTS noise. In the next sections, it is shown the device characteristics used in the numeric simulations and a correlation with the physical device, the parameters extracted through simulations and their relevance to this work, the noise curves obtained and

explanations for the events seen as the result of the simulation.

II. RTS NOISE ANALYSIS SETUP

RTS noise is observed for a small group of traps with similar characteristics, or even single traps, influencing the device expected behavior. Physical devices have different groups of traps with different characteristics and it is unlikely that, during its operation, it would be possible to isolate the traps and obtain just the RTS noise. A sum of RTS noises may be seen as a $1/f$ noise [1], been a challenge for physical measurements. Considering that, it is easier to obtain the effects of the RTS noise by simulating the device. Using numerical simulations, it is possible to isolate a group of traps, analyze its effects for just the RTS noise and study the behavior electrical behavior of the device.

The simulator used for this work is the Sentaurus Device [7]. This simulator calculates physical proprieties through different points of the device and delivers the results from a physical point of view. With that in mind, a variety of parameters are available, enabling an accurate simulation. The simulations considered the drift-diffusion transport mechanism, with models accounting for electric-field dependent mobility, bandgap narrowing and generation/recombination. Besides, the impedance field method, following the model of [8] is used for the noise calculation, which is fully determined by the trap model, not requiring adjust parameters. The models used for this work are the same as in [9,10], which shows accurate results for low frequency noise in JNTs. The results shown by this work consist in the behavior obtained for the RTS noise when varying two different parameters: trap distribution and gate voltage.

It is worth mentioning the the carriers' lifetime in such model is calculated through the fundamental Shockley-Read-Hall theory. Thus, its calculation depends on the cross section (considered as $1 \times 10^{-22} \text{ cm}^2$), carriers' concentration, temperature, trap level, trap concentration and thermal velocity.

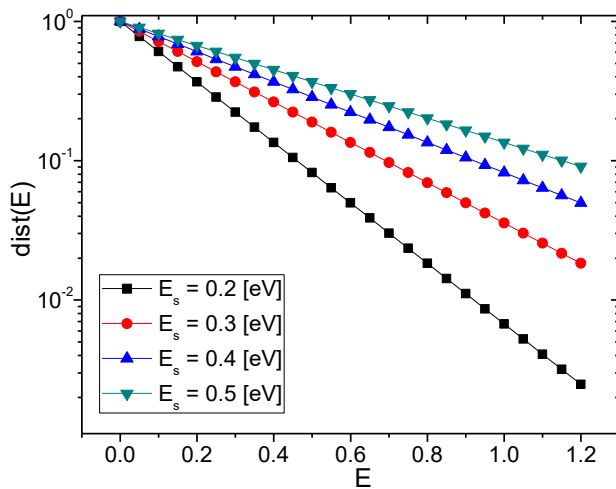


Fig. 1. Trap distribution variation according to E_s parameter, considering E_0 as zero.

III. RESULTS AND DISCUSSIONS

The trap distribution used in this work is based on an exponential, in which the maximum trap density is at the edge of the conduction band, reducing inside the badgap (typical U-shape distribution) [11]. A spatially-uniform trap density distribution has been considered within the interface between the silicon layer and the gate dielectric along the whole channel length. Sentaurus device provides a model for this kind of distribution shown below.

$$\text{dist}(E) = N_0 e^{-\left|\frac{E-E_0}{E_s}\right|} \quad (1)$$

Where N_0 is the maximum trap concentration, E_s is the distribution coefficient and E_0 is the energy of the center of energy distribution [7]. For the purpose of the simulations used in this study, the parameter E_0 will always be zero and the distribution will occur starting from the conduction band in direction to the valence band. As a reference, Figure 1 shows how the E_s coefficient impacts the distribution of traps, where the conduction band edge is at $E = 0$.

Analyzing Figure 1, it becomes evident, for lower values of E_s , the trap density decay through the bandgap will be

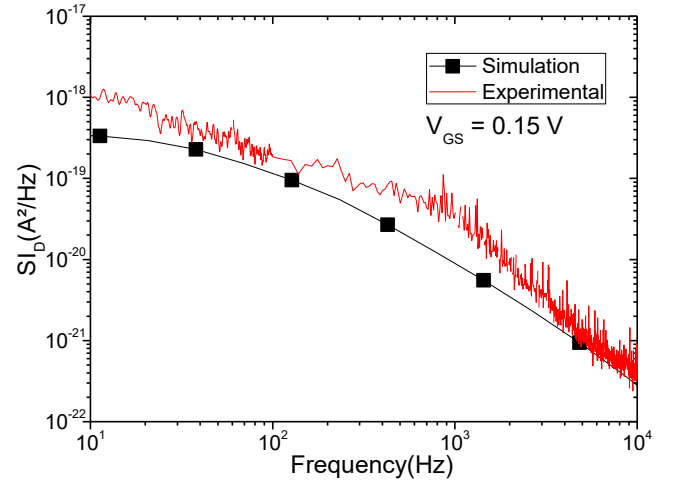


Fig. 2. Drain current noise spectral density as a function of frequency for a simulated and an experimental device.

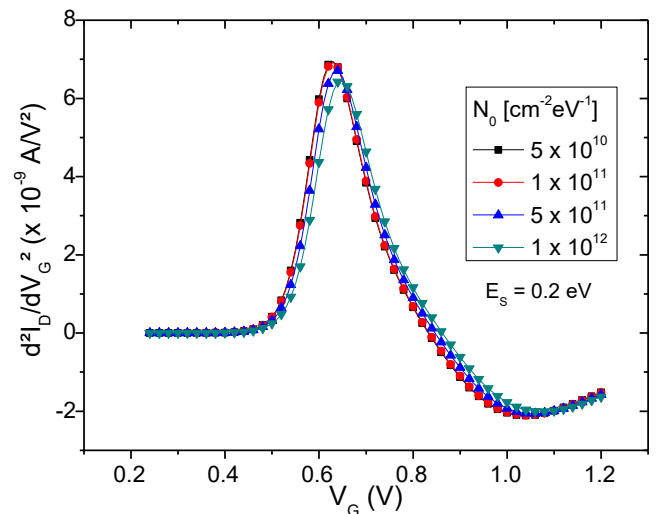


Fig. 3. Second derivative of $I_D \times V_G$ for different trap concentration.

more abrupt. This concept is essential for comprehension of the results. The total occupied traps are obtained by integrating the trap density from the valence band edge up to the surface energy level. Therefore, the closer the surface potential is to the conduction band, the higher is the number of occupied traps.

As a way to verify the accuracy of the model used for the simulations, Figure 2 presents a comparison between a simulation of the RTS noise behavior and an experimental measurement. The measured device was fabricated in CEA-Leti, according to the process described in [12]. It presents channel length of 50 nm, nanowire height and width of 10 and 20 nm, respectively, effective oxide thickness of 1.5 nm and targeted doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$, although the actual doping is expected to be of about $3.5 \times 10^{18} \text{ cm}^{-3}$ [13]. The simulated device presents similar characteristics to the experimental one.

It is noticeable that the $1/f^2$ decay is present in both measurements. The decay of the simulated curve is more defined, as it is easier to eliminate other noise components and different traps adjusting the physics of the device for the simulation, which is impossible for the physical device.

The simulated device presents width (W) and height (H) of 10 nm, channel length (L) of 100 nm, effective oxide thickness of 2nm (t_{ox}) and doping concentration (N_D) of $1 \times 10^{19} \text{ cm}^{-3}$. The first extracted parameter was the threshold voltage (V_{TH}), using the second derivative method. The second order derivative of the drain current is shown as a function of the gate voltage in Figure 3. The results were obtained for different trap concentrations (N_0) from 5×10^{10} up to $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, to analyze how interface traps could affect the V_{TH} parameter.

As the results presented on Figure 3 show, the influence of trap concentration (N_0) on the threshold voltage is very small (reduces about 30 mV for the range of N_0 variation) and was neglected throughout this work. The extracted value of V_{TH} for this device was considered as 0.64V, being this value used for all noise simulations.

The first RTS noise analysis was made with a set of different distribution coefficients (E_s). For all simulations, the device gate voltage was defined by $V_{gs} = V_{TH} + V_{gt}$, being V_{gt} the gate voltage overdrive. As V_{TH} is maintained constant, V_{gt} was the only parameter of the gate voltage that varied. The drain voltage (V_d) was defined as 50 mV.

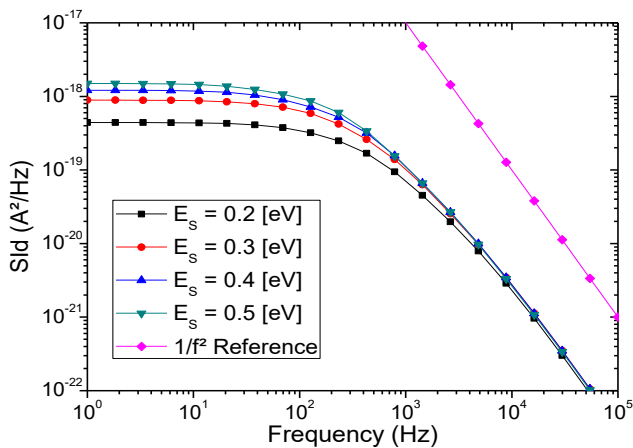


Fig. 4. Drain current noise spectral density as a function of frequency for a set of different distribution coefficients. $V_{gt} = 0,2 \text{ V}$

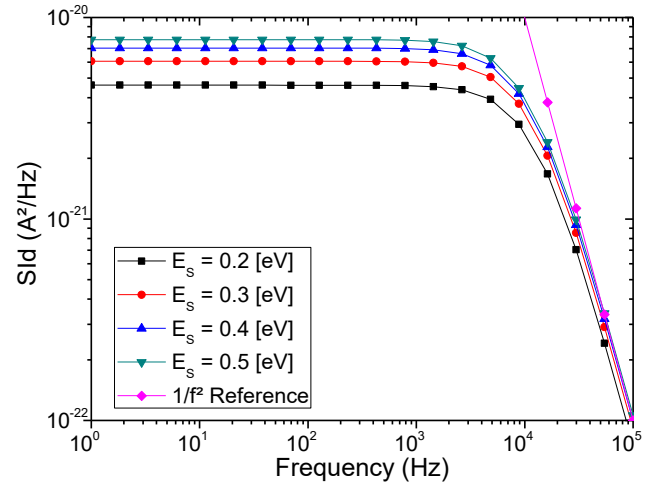


Fig. 5. Drain current noise spectral density as a function of frequency for a set of different distribution coefficients. $V_{gt} = 0,6 \text{ V}$

Figures 4 and 5 present the comparison between different distributions coefficients for two different gate voltages.

Analyzing the Figures 4 and 5 independently, it is noticeable that higher E_s generates a higher noise spectral density for f lower than the corner frequency (f_c). This effect occurs because the distribution impacts directly the concentration of traps through the energy levels inside the bandgap (which decays exponentially from the conduction band). The higher the E_s , the larger the amount of traps in the bandgap. This effect is noticeable in both Figures.

Comparing the curves of both figures, it is observed that two parameters are altered, the corner frequency and the initial noise spectral density. This effect is explained as the noise is also correlated with the electric field and not only with the traps. The equation (2) [14] can be used to better understand how the relation occurs.

$$S_{vg} = n_{Nit} \Delta V^2 f_0(E) (1 - f_0(E)) \frac{4\tau(E)}{1 + (2\pi f\tau(E))^2} \quad (2)$$

In Eq. 2, where n_{Nit} is the number of traps that contributes for the noise, ΔV is the voltage variation that occurs in function of the capture and emission of one charge by the trap and τ is the carriers' lifetime. So that, the corner frequency is related to the capture and emission times through τ , which is given by expression (3), where τ_C and τ_E are the capture and emission times, respectively.

$$\tau = (\tau_C^{-1} + \tau_E^{-1})^{-1} \quad (3)$$

As the gate voltage increases, all the parameters mentioned before are altered. n_{Nit} depends on the surface potential and, as the gate voltage increases to the flatband, the surface potential is reduced. Above V_{FB} , the surface potential maintains an almost constant behavior. ΔV depends on the gate oxide capacitance. τ depends on the charges in the conduction layer and on the electric field. As the electric field varies in direction of V_{FB} , τ decreases. Consequently, the initial noise spectral density for the curves gets altered to lower values and the corner frequency increases. Following this analysis, it is possible to see that the effects of τ in the noise behavior of the device is considerably stronger than the other variables in the equation.

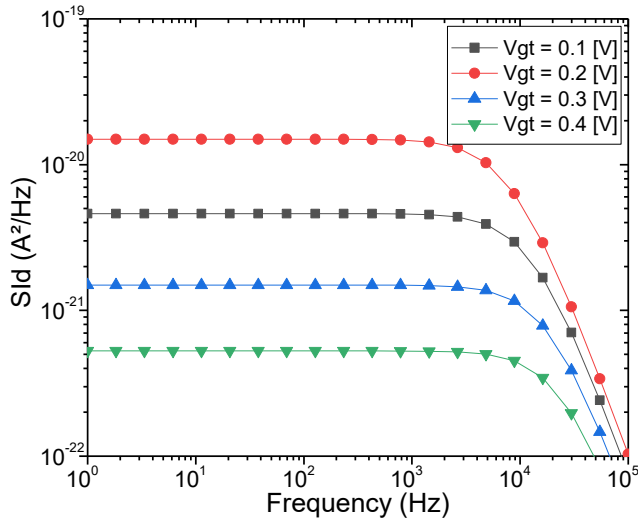


Fig. 6. Drain current noise spectral density as a function of frequency for a set of V_{gt} from 0.1V to 0.4V.

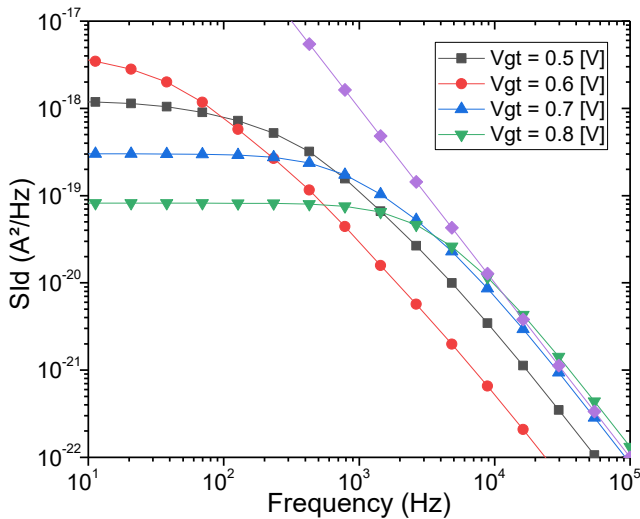


Fig. 7. Drain current noise spectral density as a function of frequency for a set of V_{gt} from 0.5V to 0.8V.

A second set of curves obtained were separated in two parts, below and above V_{FB} . The flatband voltage is calculated by equation (4).

$$V_{FB} = -\frac{Q_{SS}}{C_{OX}} + \phi_{MS} \quad (4)$$

The results obtained in Figure 6 shows that the main variation while altering V_{gt} , i.e. when the conduction occurs only by the center of the device, without the formation of the accumulation layer, is the shift in the S_{id} plateau level observed for lower frequencies. So that, it is easily predictable, showing a uniform behavior. Corroborating with that, the corner frequency shows almost no variation with V_{gt} , indicating that the carriers' lifetime does not suffer a significant variation.

When comparing Figure 6 (lower v_{gt}) to Figure 7 (larger V_{gt}), a different scenario is observed, where the behavior is non-linear, and a correlation between the curves in Figure 7

is not easily seen. Equation (2) may elucidate the phenomena involved. As the accumulation is increased, the electron concentration in the device accumulation region increases. In this case, the carriers' lifetime is reduced, which increased the corner frequency with V_{gt} . Besides that, the electrons' lifetime decrease lowers the noise plateau.

IV. CONCLUSIONS

This work has evaluated the behavior of the RTS noise in junctionless transistors considering different gate voltages and the exponential decay factor, which indicates the exponential trap profile along the conduction band, i.e. a maximum amount of traps is considered in the conduction band and decays exponentially to the valence band. Through the overall analysis, it was possible to identify two peculiar behaviors of the RTS noise when the device was biased in partial depletion and in accumulation. In partial depletion, a noise plateau was obtained at lower frequencies followed by a corner frequency and a $1/f^2$ noise decay. Such frequency presents low dependency on the gate voltage, which can be understood as a nearly gate voltage-independent carriers' lifetime. When biased in accumulation, on the other hand, it could be observed a reduction in the plateau level with the gate voltage increase as well as an increase in the corner frequency, indicating a reduction in the carriers' lifetime.

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REFERENCES

- [1] M.V. Haartman, M. Östling, *Low-Frequency Noise in Advanced MOS Devices*, Springer, 2007.
- [2] J.-P. Colinge, C.-W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain et al., "SOI gated resistor: CMOS without junctions", In: *Proceedings of IEEE International SOI Conference*, 2009, pp. 1–2.
- [3] R.T. Doria, R. Trevisoli, M. de Souza, M.A. Pavanello, "Low-frequency noise and effective trap density of short channel p- and n-types junctionless nanowire transistors", *Solid-State Elect.*, vol. 96, pp. 22–26, 2014.
- [4] D.-Y. Jeon, S.J. Park, M. Mouis, S. Barraud, G.-T. Kim, G. Ghibaudo, "Low-frequency noise behavior of junctionless transistors compared to inversion-mode transistors", *Solid-St. Electron.*, vol. 81, pp. 101–104, 2013.
- [5] D. Jang, J.W. Lee, C.-W. Lee, J.-P. Colinge, L. Montès, J.I. Lee, G.T. Kim and G. Ghibaudo, "Low-frequency noise in junctionless multigate transistors", *App. Physics Letters*, vol. 98, pp. 133 502, 2011.
- [6] P. Singh, N. Singh, J. Miao, W.-T. Park and D.-L. Kwong, "Gate-All-Around Junctionless Nanowire MOSFET with Improved Low-Frequency Noise Behavior", *IEEE Elec. Dev. Lett.*, vol. 32, pp. 1752–1754, 2011.
- [7] Sentaurus Device User Guide, Synopsys, Mountain View, CA, USA, 2016.
- [8] F. Bonani and G. Ghione, "Generation-recombination noise modelling in semiconductor devices through population or approximate equivalent current density fluctuations", *Solid-State Electron.*, vol. 43, no. 2, pp. 285–295, 1999.
- [9] R. Trevisoli, R.T. Doria, S. Barraud, M. Pavanello. Compact Analytical Model for Trap-Related LowFrequency Noise in Junctionless Transistors. In: *ESSDERC 2019 - 49th European Solid-State Device Research Conference*, pp. 1–4, 2019.

- [10] R. Trevisoli, M.A. Pavanello, C.E. Capovilla, S. Barraud, R.T. Doria, "Analytical Model for Low-Frequency Noise in Junctionless Nanowire Transistors", *IEEE Trans. Electron. Dev.*, v. 67, pp. 2536-2543, 2020.
- [11] E.H. Nicollian and J.R. Brews, *MOS Physics and Technology*, Wiley, 1982.
- [12] S. Barraud et al., "Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1225–1227, Sep. 2012.
- [13] R. Trevisoli; R.T. Doria; M. de Souza; S. Barraud; M.A. Pavanello; "A New Method for Junctionless Transistors Parameters Extraction"; In: *ESSDERC 2017 - 47th European Solid-State Device Research Conference*, pp. 1-4, 2017.
- [14] R. Trevisoli, R.T. Doria, S. Barraud, M.A. Pavanello, "Modeling the interface traps-related low frequency noise in triple-gate SOI junctionless nanowire transistors", *Microelectronic Engineering*, v. 215, pp. 111005, 2019.