Performance of OCTO Layout Style on SOI MOSFET Switches under High-temperature Operation

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***Abstract*—The present paper performs an experimental comparative study of the main switching electrical parameters and figures of merit of the octagonal layout style for the planar Silicon-On-Insulator (SOI) Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFET), named Octo SOI MOSFET (OSM), in comparison with the typical rectangular one, regarding a large range of temperature, varying from 300 K to 573 K. The devices were manufactured in a 2 µm fully-depleted SOI (CMOS) technology and are n-type. The results have shown that the OSM is capable of keeping active the Longitudinal Corner Effect (LCE), PArallel Connection of MOSFETs with Different Channel Lengths Effect (PAMDLE) and Deactivate the Parasitic MOSFETs of the Bird's Beak Regions Effect (DEPAMBBRE), which are intrinsic effects of the gate octagonal structure of the MOSFET. Besides, it is able to present a higher electrical performance as compared to its rectangular SOI MOSFET (RSM) counterpart (same channel width and bias conditions). As an illustration, the OSM on-state drain current (I_{ON}) and off-state drain current (I_{OFF}) are respectively 186% higher and 64% smaller as compared to those found in its RSM counterpart.**

***Index Terms*— New layout styles; Octo layout style; high-temperature environment; LCE, DEPAMBBRE and PAMDLE effects.**

I. INTRODUCTION

Electronics face great challenges in order to be able to operate in harsh environments (high-temperature, ionizing radiation, etc.), aiming at the reduction of the short channel effects by taking into account the MOSFETs scaling, the decrease of the drain leakage current (I_{LEAK}) and power consumption, the diminution of the variations of mobilities of mobile charge carriers in the channel, etc. [1-3].

Several areas of the industry need new electronic systems that must operate reliably under such harsh environments. For example, the exploration and monitoring of the oil, gas and geothermal wells use probes that are sent deep into bore holes, with temperatures reaching 473 K to 573 K (200 ºC to 300 ºC). Other applications include instrumentation for engines, engine control and condition monitoring systems, power conditioning and control systems for space platforms and satellites, nuclear reactor instrumentation and control, as well as automotive and aeronautics electronics and integrated sensors [1-4].

Many factors determine the practical upper temperature limit of semiconductor devices that does not reflect the inherent temperature limit of the semiconductor materials. The practical limit is frequently determined by the electrical properties of the used semiconductor materials, the interconnections and packaging, both for active devices and passive components [3, 4]. As an indication of the practical upper limit, Bulk Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) have long been offered commercially for operations reaching a maximum of 423 K (150 ºC). Temperature up to 473 K-493 K (200-220 °C) can be reached with specific Bulk CMOS process and circuit designs [1, 2].

Other technologies have then been studied to improve the performance of electronic systems operating at high temperatures, such as Fin Field-Effect Transistors (FinFET) built in Silicon-on-Insulator (SOI) processes which have demonstrated a good electrical performance at high temperatures thanks to their gate double structure [5, 6]. Besides, the use of Gate-All-Around (GAA) MOSFET devices in digital CMOS ICs is able to keep the silicon layer fully depleted at extremely high-temperatures [7].

For temperatures above 573 K (300 ºC) and, theoretically, up to 873 K (600 ºC), silicon carbide (SiC) attracted the attention of the researchers due to its unique electrical and thermo-physical properties. It has a wide bandgap energy (2.2 eV to 3.3 eV, depending on the polytype of SiC), a significantly higher thermal conductivity for thermal management of high-power devices, a high critical breakdown electric field for large power output, a reduced I_{LEAK} in MOSFETs, etc. [3, 8-10].

The technology based on 4H-SiC semiconductors utilizes the unique physical and electrical properties of this electrical material to achieve improved performance in high-power and high-temperature electronic circuits [11]. Their complexity nevertheless remains limited due to the lesser integration density and scalability reached in SiC processes as compared to the Si CMOS [11].

The Silicon-On-Insulator (SOI) CMOS technology presents an excellent behavior at high temperatures. When operated in a temperature range from 398 K (125 ºC) to 573 K (300 ºC), the devices implemented in SOI CMOS technology presents three major advantages as compared to conventional Bulk MOSFETs: the first is the suppression of latch-up; the second is the reduction of I_{LEAK} and the third, a smaller variation of threshold voltage (V_{TH}) with the temperature [2, 12, 13]. Besides, the devices manufactured with SOI CMOS technology further enables high scaling, integration density and production levels. Consequently, this technology has been chosen in this study [2, 12, 13].

Therefore, by mixing the best electrical characteristics of SOI MOSFETs at elevated temperatures and by applying the PN junctions engineering among the source/channel/drain regions or simply gate layout changing of MOSFETs, it is possible to insert novel effects that are capable of improving their electric performances. These new effects are: LCE, PAMDLE, DEPAMBBRE [14-19] that are able to boost its electrical performance. Some examples of this approach are the Diamond [14-22], Octo [23-27], Ellipsoidal [28] and Fish [29] layout styles for MOSFETs, which are capable of

Digital Object Identifier 10.29292/jics.v14i2.34

reaching these challenging goals.

The Octo layout style for MOSFETs was specially invented in order to further boost the Electrostatic Discharge (ESD) tolerance and increase the breakdown voltage (BV_{DS}) as compared to those one found in the Diamond (hexagonal gate shape) layout style. The same effects found (LCE, PAMDLE and DEPAMBBRE) in the Diamond SOI MOSFET also exist in the OSM structure, in which the LCE in the OSM structure is more pronounced, because in this case, it is possible to find a higher resultant longitudinal electric field (LEF). This can be justified due to the presence of three longitudinal electric field components instead two of the Diamond SOI MOSFET [21-27].

Several references about the Octagonal SOI MOSFET (OSM) describe its better performance in terms of saturation drain current (I_{DS}), transconductance (gm), gm/I_{DS} ratio, voltage gain (A_V), unit voltage gain frequency (f_T), R_{ON}, I_{LEAK}, I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio, as compared to those observed in the rectangular SOI MOSFET (RSM) counterparts, regarding the same gate areas (A_G) and bias conditions in room-temperature environments [14-27].

Four prior experimental studies describe in detail the better electrical performance of the DSM [14, 30] and OSM [31, 32], mainly regarding analog CMOS ICs applications operating at high-temperature environment, in relation to the traditional rectangular MOSFET counterpart.

Within this context, this manuscript aims at studying the electrical performance of the main parameters and figures of merit (I_{ON}, I_{OFF}, I_{ON}/I_{OFF} Ratio and On-State Resistance (R_{ON})) of the Octo layout style (OLS) for n-type SOI MOSFET switches in relation to the rectangular counterpart in a large range of temperature varying from 300 K to 573 K (27 ºC to 300 ºC), regarding the same channel width (W) and bias conditions.

II. Device's Characteristics and Structures

Fig. 1 illustrates the top views of the OSM (Fig. 1.a) and its corresponding RSM (Fig. 1.b), regarding the same channel width and A_G. In Fig. 1.a, W is the channel width, B and b are the largest and smallest channel lengths, respectively, B' is the height of the triangle part of the hexagonal gate geometry, W_T is the height of the trapezoidal part that composes the octagonal gate shape which is equal to $\left(\frac{B-b}{2}\right)\tan\left(\frac{\alpha}{2}\right)$, W_R is equal to (W-2W_T), which is the channel width of the rectangular part that composes its gate octagonal geometry, α is the angle formed by the triangular part of the hexagonal geometry of the gate octagonal region, X means the lengths of the drain/source regions, the resultant LEF at the point P of the OSM due to the drain bias (V_{DS}) is $\overrightarrow{\varepsilon_{//\_OSM}}$, which is given by the vectorial sum of three LEF components, $\overrightarrow{\varepsilon_{//1}}$, $\overrightarrow{\varepsilon_{//2}}$ and $\overrightarrow{\varepsilon_{//3}}$ (LCE effect) that are perpendicular to the interfaces composed by the drain/source and the silicon film regions [21, 26], L is the RSM channel length and the $\overrightarrow{\varepsilon_{//\_RSM}}$ is the LEF of the RSM (only one LEF component).

Considering the point P in these two transistors (Fig. 1), the OSM provides a higher longitudinal electric field ($\overrightarrow{\varepsilon_{//\_OSM}}$) than the one found in the RSM counterpart ($\overrightarrow{\varepsilon_{//\_RSM}}$) due to the LCE effect, regarding the same A_G, W and bias conditions. The OSM structure is created when we cut the extreme corners of the diamond SOI MOSFET by a factor "c" (Fig. 1.a) in order to improve the LCE, the electrostatic discharge (ESD) robustness, increase the BV_{DS} and the I_{DS} [23-25].

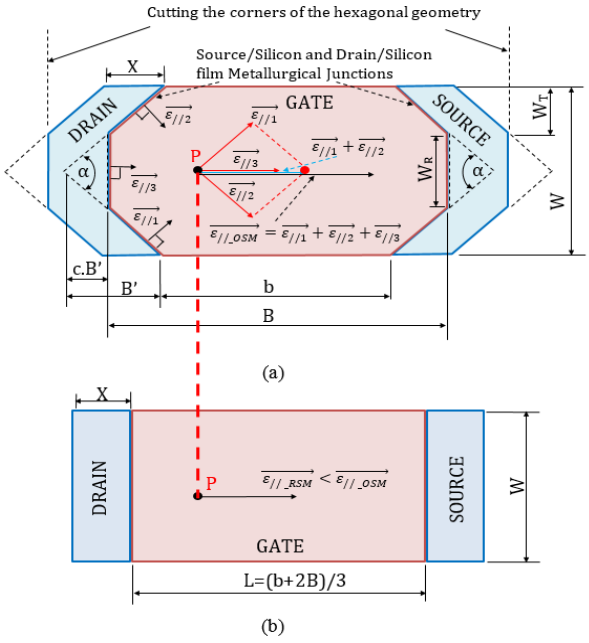

Fig.1 Top schematic views of the OSM (a) and its RSM counterpart (b), regarding the same gate, W and its corresponding longitudinal electric field components.

The channel length (L) of an RSM must be equal to $\left(\frac{2B+b}{3}\right)$ in order for it to have the same gate area of an OSM. The effective channel length (L_{eff}) of an OSM, due to the PAMDLE effect, is given by Equation (1) [24]:

$$L_{eff} = \frac{1}{\left(\frac{1-c}{B-b}\right)ln\left(\frac{B}{b}\right)+\frac{c}{B}} \quad (1)$$

Regarding the same gate areas of the OSM and RSM, the OSM L_{eff} is smaller than the RSM L [24]. Therefore, the octagonal layout style for MOSFETs is capable to present a higher I_{DS} than the one observed in the RSM equivalent, regarding the same bias conditions [19].

The novel effects (LCE, PAMDLE and DEPAMBBRE) take place simultaneously in the OSM and they are responsible for uplifting its electrical performance in relation to the its RSM counterpart [19].

The dimensional characteristics of the OSM and their RSM counterparts used to perform the experimental work are indicated in Table I and all devices present the same channel width equal to 30 µm.

The parameters studied in this paper have been normalized by the aspect ratio (W/L) in order to avoid the influence of the difference of the devices' dimensions (Table I). The channel length (L*) of the OSM used to perform the normalizations of the electrical parameters and figures of merit is given by the equation $L^* = \left(\frac{2B+b}{3}\right)$, which corresponds to an L of an RSM counterpart which presents the same gate area than the one found in the OSM.

Table I. Dimensions of the devices used for this experimental study (W=30 μm and b=5 μm).

	SOI nMOSFETs					
	OSM1	RSM1	OSM2	RSM2	OSM3	RSM3
α (°)	53.1	-	90.0	-	126.9	-
B (μm)	50.0	-	27.5	-	16.5	-
L* (μm)	35.0	-	20.0	-	12.7	-
L_{eff} (μm) (PAMDLE)	23.0	-	15.20	-	10.75	-
$(W/L)_{OSM}$	0.86	-	1.5	-	2.37	-
Dimension of PN junction between drain and channel regions (μm)	57.8	30.0	39.3	30.0	32.7	30.0
$(W/L)_{RSM}$	-	1.09	-	1.85	-	2.78
L (μm)	-	27.5	-	16.25	-	10.8
A_G (μm^2)	994	825	572	487.5	363	324

We have used three pairs of SOI MOSFETs as follows:

• An OSM (α=53.1°), named OSM1, and its RSM equivalent (RSM1). The OSM L* is equal to 35 μm, which corresponds to $L^* = \left(\frac{2B+b}{3}\right)$ of an RSM counterpart, with the same gate area of the OSM. However, the OSM L_{eff} [Equation (1)] is 14% smaller (PAMDLE Effect) than the one found in the RSM counterpart.

• An OSM (α=90.0°), named OSM2, and its RSM equivalent (RSM2). The OSM L* is equal to 20 μm, which corresponds to L of an RSM counterpart, with the same gate area of the OSM. However, the OSM L_{eff} is 7% smaller (PAMDLE Effect) than the one in the RSM counterpart.

• An OSM (α=126.9°), named OSM3, and its RSM equivalent (RSM3). The OSM L* is equal to 12.7 μm, which corresponds to L of an RSM counterpart which presents the same gate area of the OSM. Note that its OSM L_{eff} is practically the same from the RSM counterpart, because in this case the PAMDLE effect is practically trivial.

The SOI MOSFETs were manufactured in Microelectronics Laboratory of the Université Catholique de Louvain, Belgium. The fully-depleted SOI CMOS manufacturing process used was of 2 μm, notably optimized for high-temperature operation and analog applications at voltages higher than 3 V. The main technological parameters of these SOI MOSFETs are: the gate oxide thickness (t_{ox}), the silicon film thickness (t_{Si}), and the buried oxide thickness (t_{Box}) are equal to 30 nm, 80 nm and 390 nm, respectively. The concentrations of acceptors impurities in the channel region is $6x10^{16}$ cm^{-3} and the donors impurities in the regions drain and source are equal to $1x10^{20}$ cm^{-3} [31, 32].

III. Experimental results and discussion

This section presents comprehensive analytical and experimental results of the switching electrical parameters and figures of merit, taking into account the high-temperature effects, in a range from 300 K to 573 K. The SOI MOSFETs are of n-type, Fully Depleted (FD) and the bias applied to the back-gate is equal to zero, i.e. the second interface is in depletion.

A. On-state drain current (I_{ON})

The On-State Drain Current (I_{ON}) is defined as the drain current that is measured in the strong inversion region, in which the SOI MOSFET is operating with gate voltage (V_{GS}) values greater than V_{TH} [33].

The high temperatures have a great influence on the MOSFET I_{DS} and consequently on its I_{ON}. The mobilities of electrons and holes depend, mainly, on the impurity concentrations and the temperature that the semiconductor is exposed to [2, 34, 35]. The flow of the mobile charge carriers in a semiconductor is limited by scattering mechanisms (lattice scattering and impurity scattering) which strongly reduce their mobilities (μ) depending on the temperature. Thus, as the temperature increases, the thermal agitation increases and, consequently, the mobile charge carriers are further scattered in the lattice, and therefore their mobilities are reduced. This phenomenon leads to the reduction of I_{DS} in a MOSFET exposed at high temperatures in strong inversion [34, 35].

Besides, the phonon scattering is capable of limiting the mobilities of mobile charge carriers in the channel (μ_{ph}) at high temperatures, knowing that these mobilities are reduced proportionally to T^{-m}, with m being typically close to 1.5 regarding a n-type SOI MOSFET [2, 34, 35].

To illustrate the effect that the temperature increase, in a range of the temperature from 300 K to 573 K, causes on the I_{DS} of a SOI MOSFET, we have presented in Fig. 2.a the experimental curves of I_{DS} normalized by the aspect ratio (W/L) as a function of V_{GS} in linear and logarithm scales, regarding V_{DS} equal to 5 V. Fig. 2.b shows the I_{DS}/(W/L) as a function of the V_{DS}, considering the gate voltage overdrive (V_{GT}=V_{GS}-V_{TH}) equal to 1 V.

By analyzing Fig. 2, we observe that the I_{DS}/(W/L), for all devices, have reduced with the temperature increase, as previously explained [2, 34, 35].

In the triode region (Fig. 2.a), regarding V_{GS} and V_{DS} equal to 3 V and 5 V, respectively, the OSM2 I_{DS}/(W/L) presents a gain of 61%, 97% and 66% in relation to I_{DS}/(W/L) of the its RSM counterpart, regarding the temperature equal to 300 K, 423 K and 523 K, respectively. For the saturation region (Fig. 2.b), regarding V_{DS} and V_{GT} equal to 3 V and 1 V, respectively, the OSM2 I_{DS}/(W/L) is always higher (by approximately 67%, 63.8% and 76%, regarding the temperature equal to 300 K, 423 K and 523 K, respectively) than those observed in its RSM counterparts. Therefore, the octagonal layout style for SOI MOSFETs is capable of maintaining the LCE and PAMDLE for high temperatures considered in this experimental study.

In addition, we have observed that the V_{TH} of all SOI MOSFETs also vary with increasing temperature. This variation can be observed in Fig. 3, in which the method of extraction of V_{TH} used was through the maximum peak of the second derivative of the curve I_{DS}/(W/L) as a function of V_{GS}, for V_{DS} equal to 100 mV [2, 34].

By analyzing Fig. 3, we can see that the V_{TH} of all SOI MOSFETs reduces linearly by about 1 mV/°C, in first approximation, as the temperature increases [34] and therefore the I_{ON} and I_{OFF} also are affected by the temperature, because both are strongly influenced by V_{TH}

[34, 36]. But, in this study the variations of V_{TH} as temperature increases have not influenced the $I_{ON}/(W/L)$ values, because the $I_{ON}/(W/L)$ values are extracted as a function of V_{GT} (the use of V_{GT} eliminates the differences of the V_{TH} found in the different MOSFETs).

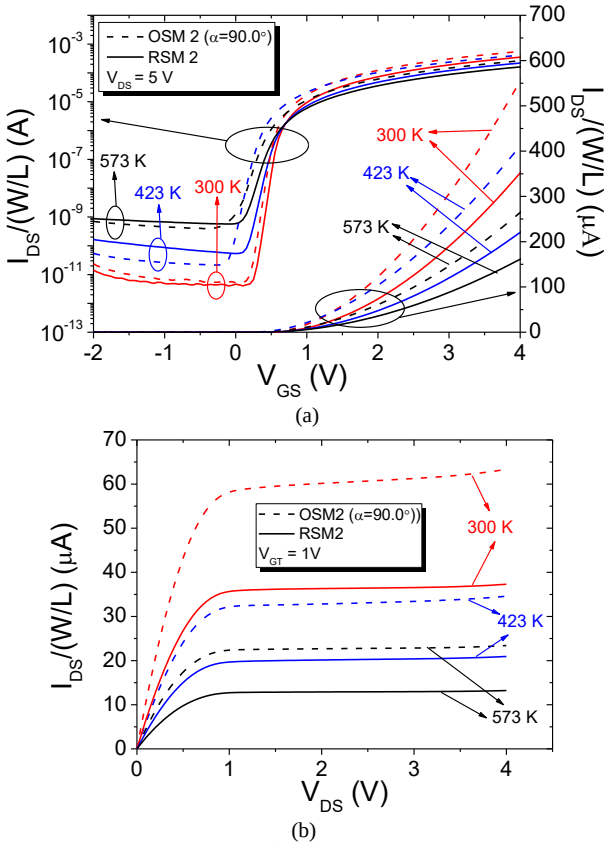

Fig.2 Experimental curves of the OSM2 $I_{DS}/(W/L)$ and its RSM counterparts as a function of V_{GS} (a), in linear and logarithm scales and V_{DS} (b), in which they show the reduction of $I_{DS}/(W/L)$ with the temperature increase in both devices.

The experimental curves of the $I_{ON}/(W/L)$ as a function of the temperature (T) of the OSM and their RSM counterparts, regarding V_{GT} equal to 4 V and V_{DS} equal to 100 mV in triode region are presented in Fig. 4 (Fig. 2.a shows another example of the variation of $I_{ON}/(W/L)$ with the temperature).

Fig. 4 shows that the OSM $I_{ON}/(W/L)$, with different α angles, is always higher (by approximately 118%, 58% and 25% for 300 K, and 186%, 60% and 28% for 573 K, regarding α angles equal to 53.1º, 90.0º and 126.9º, respectively) than the ones observed in their RSM counterparts for all considered temperatures. This can be justified due to the occurrence of LCE, PAMDLE and DEPAMBBRE effects in the OSM structures.

Besides, we can see that LCE, PAMDLE and DEPAMBBRE effects are kept active in high-temperature conditions (up to 573 K). Although, the density of mobile charge carriers in the conduction band increases with temperature, we note that the $I_{ON}/(W/L)$ of the devices reduces when the temperature increases. This happens mainly due to the reduction of the mobility of mobile charge carriers in the channel region when the temperature increases [2, 34, 35].

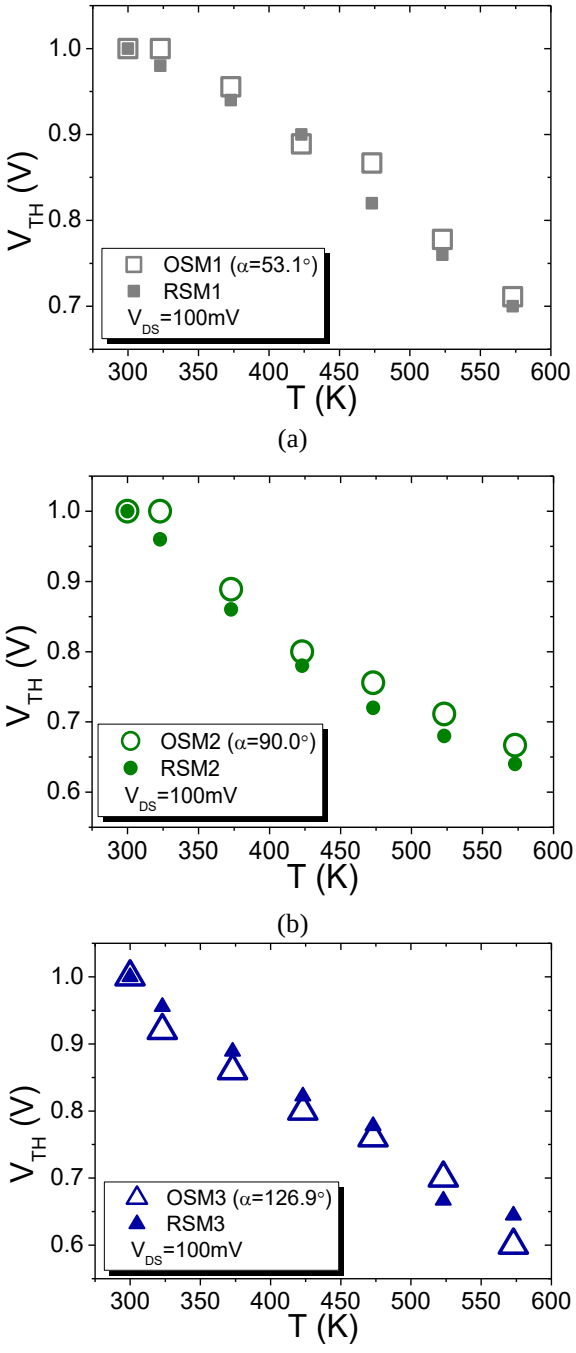

Fig.3 Curves of all SOI MOSFET V_{TH} as a function of temperature, regarding different α angles of the OSM [53.1º (Fig. 3.a), 90º (Fig. 3.b), and 126.9º (Fig. 3.c)] and their respective RSM counterparts.

When the α angle of the OSM increases, its gain in the $I_{ON}/(W/L)$ decreases due to the reduction of the LCE and PAMDLE effects. Besides, the OSM is increasingly approaching a structure with rectangular gate geometry (RSM).

An interesting fact that the Fig. 4 shows us is that, when normalized by the aspect ratio, the RSM $I_{ON}/(W/L)$ is similar for the three RSM, contrarily to what occurs in the three OSM, due the effects LCE, PAMDLE and DEPAMBBRE.

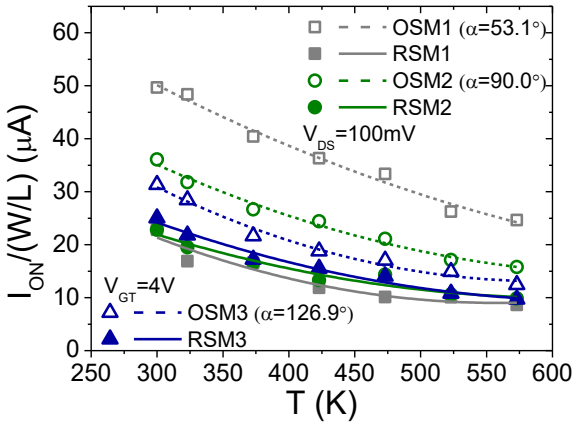

Fig.4 Experimental curves of the OSM I_{ON}/(W/L) with three different α angles and their RSM counterparts as a function of T.

These effects are responsible for boosting the device electrical performances, which are related to the value of the α angle of the octagonal gate shape of the OSM. Therefore, when the α angle decreases from 126.9º to 53.1º, for example, these effects are increased in the OSM structure and, consequently, the OSM that presents the smallest α angle tends to present a higher electrical performance than those that present greater α angles values. Because of this, the OSM1, with α angle equal to 53.1º, presents a higher value of I_{ON}/(W/L), for all temperatures considered, than those of the OSM2 with a α equal to 90º and OSM3 with a α equal to 126.9º, respectively.

Based on these I_{ON}/(W/L) results of the OSM in relation to their RSM counterparts, the octagonal layout style for SOI MOSFETs can be considered an interesting alternative to be used in digital SOI CMOS ICs applications, either to boost the current drive by fixing the die area of SOI CMOS ICs or to reduce the total die area of analog SOI CMOS ICs, regarding the same current drive [33, 36].

B. Off-state drain current (I_{OFF})

The I_{OFF} is given by the MOSFET drain current for V_{GS} equal to 0 V and V_{DS} near to the supply voltage (V_{DD}). These bias conditions define the MOSFET operating as an open switch. As can be seen in Fig. 2.a, in our case, this drain current is not influenced by the subthreshold slope, but at low V_{DS}, it is generated in the depletion regions of the reverse-biased PN junctions which are defined by the drain/source and channel regions [34, 37].

A Fully Depleted (FD) SOI MOSFET with the second interface in depletion presents an I_{OFF} smaller than the one found in the Conventional (Bulk) MOSFET under high temperatures. This happens as the FD SOI MOSFET presents smaller areas of the PN junctions of the drain/source and channel interfaces than those observed in the Bulk MOSFET and due to elimination of large well-to-substrate diffusion leakage. It is important to highlight that I_{OFF} is considered a leakage drain current in digital SOI CMOS ICs applications [34, 37].

The I_{OFF} in a SOI MOSFET is, basically, comprised of two components [37]:

I - The generation current in the depleted region of the reverse-biased drain junction (I_{ger});

II - The diffusion current from the undepleted part of the Si film (I_{diff}).

The I_{ger} in the drain region in the n-channel SOI MOSFET can be given by Equation (2) [37]:

$$I_{ger} = q\, t_{Si} W \frac{n_i}{\tau_g}\left\{\sqrt{\frac{2\,\varepsilon_{Si}\,k\,T}{q^2\,N_A}}\left[\sqrt{\ln\left(\frac{N_A}{n_i}\right)+\frac{q\,V_{DS}}{k\,T}}-\sqrt{\ln\left(\frac{N_A}{n_i}\right)}\right]\right\} \qquad (2)$$

where q is the electron charge, t_{Si} is the silicon film thickness, W is the device width, n_i is the intrinsic carrier concentration, τ_g is the generation lifetime, N_A is the channel doping, T is the temperature in Kelvin, k is the Boltzmann constant and ε_{Si} is the permittivity of silicon [37].

The I_{diff} in n-channel enhancement-mode SOI MOSFET can be expressed by the Equation (3) [37]:

$$I_{diff} = q\, W \sqrt{\frac{D_n}{\tau_{rn}}}\left(1-e^{-\frac{q\,V_{DS}}{k\,T}}\right)\int_0^{t_{Si}}\left(\frac{n_i^2}{N_A}\, e^{\frac{q\,\varphi(x,T)}{k\,T}}\right)dx \qquad (3)$$

where D_n is the electron diffusion constant, τ_{rn} is the electron recombination lifetime (equal to L_n^2/D_n, in which L_n is the electron diffusion length [33]) and φ(x,T) represents the potential distribution across the film thickness in the undepleted Si film [37].

According to Equation (3), we can note that the I_{diff} in an SOI MOSFET is determined by the distribution of the potential and by the concentration of minority charge carriers, which vary with the gate bias and the silicon layer thickness (Si). In addition, the concentration of minority charge carriers in the channel region can be reduced by the increase, in modulus, of the back-gate negative voltage in a SOI nMOSFET, thereby reducing the off-state diffusion current and, thus, I_{OFF} [37].

The dependency of the I_{OFF} with the temperature is related to the intrinsic charge carrier concentration. For temperatures below 423 K and high V_{DS}, the I_{OFF} follows the variation of n_i with the temperature, indicating predominance of the current generation effect [36]. At temperatures above 423 K, the I_{OFF} follows the variation of n_i^2 with the temperature, suggesting that the diffusion mechanism is dominant [37]. Therefore, the I_{OFF} increases with the rising temperature.

The I_{OFF} is a parameter of utmost importance for the SOI CMOS ICs with very low power consumption, when the SOI MOSFETs is operating in the cut-off region [2, 33].

To obtain the I_{OFF}, the SOI MOSFET is biased with V_{GS} equal to zero and high value of V_{DS}, i.e., cutoff region [20] (Fig. 2.a) shows an example of the variation of I_{OFF}/(W/L) with the temperature). Fig. 5 illustrates the experimental curves of the I_{OFF}/(W/L) as a function of the T of the OSM and their RSM counterparts, for a V_{GS} equal to 0 V and a V_{DS} equal to 5 V (cutoff region).

Analyzing Fig. 5, the OSM with α equal to 126.9º and its RSM counterpart present I_{OFF} in the same order of magnitude for all temperatures considered. Because, for this angle the octagonal gate geometry of the OSM is very close to the rectangular, resulting in similar values of the PN junctions areas and lengths between the drain and channel depletion regions for both devices.

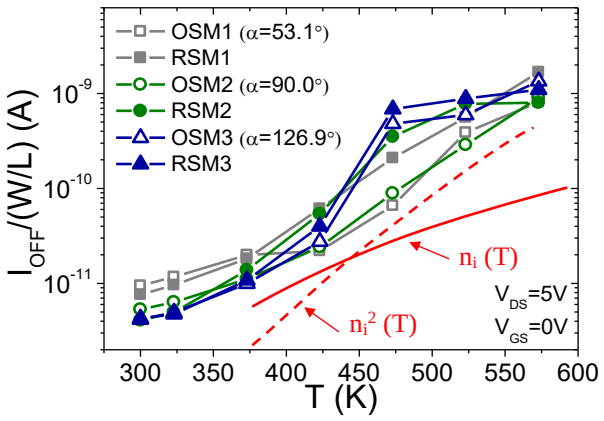

Fig.5 The experimental I_{OFF}/(W/L) of the OSM and their RSM counterparts as a function of T, red lines show physical trends.

When the temperature is between 300 K and 373 K, the I_{OFF} values to the OSM1 and OSM2 can be seen to be slightly higher than those found in the OSM3 and their respective RSM counterparts and to increase with α reduction. However, above the temperature of 423 K, where the diffusion current is prevailing [36], the I_{OFF} of the OSM1 and OSM2 are always lower (approximately 64% and 55% for 423 K, and 53% and 13% for 573 K, with α angles equal to 53.1º and 90.0º, respectively) than those found in their RSM counterparts, as well as compared to OSM3, considering the same bias conditions.

One hypothesis to explain these results is that, below 373 K the generation I_{OFF} dominates and is linked to the electrical field in the depletion region which increases in the OSM.

On another hand, at higher temperatures, the diffusion I_{OFF} is known to be inversely proportional to the diffusion lengths (L_n and L_p), according equation (4) [34] (from the standard PN junction theory).

$$I_{OFF} = A\left(\frac{qD_n\, n_{p0}}{L_n} + \frac{qD_p\, p_{n0}}{L_p}\right) = Aqn_i^2\left(\frac{1}{N_A}\sqrt{\frac{D_n}{\tau_{rn}}} + \frac{1}{N_D}\sqrt{\frac{D_p}{\tau_{pn}}}\right) \qquad (4)$$

where A is the area of the drain to channel PN junction, n_{p0} is the equilibrium electron concentration in the p-type region, D_p is the hole diffusion coefficient, p_{n0} is the equilibrium hole concentration in the n-type region, L_p is the hole diffusion length and τ_{pn} is the hole recombination lifetime (equal to L_p^2/D_p) [34]. As the main effect of the OSM angle reduction is to increase the longitudinal electrical field, it can only impact the diffusion current through second-order effects, such as the reduction of diffusion coefficients through mobility, given by the Einstein Relationship [D_n=(kT/q).μ_n] [34], another possibility could be the balance of the diffusion by a drift current component. This should be studied in details in future works by three-dimensional (3D) numerical simulations.

C. I_{ON}/I_{OFF} Ratio

The electrical performance and processing velocity of digital CMOS switches, which operate at high frequencies, is directly related with the I_{ON}/I_{OFF} ratio [32].

The I_{ON}/I_{OFF} ratio decreases with the increase of the temperature, because the increase of I_{OFF}/(W/L) at high temperatures is more significant (it depends on n_i^2 – Section III.B) than the reduction in I_{ON}/(W/L) (which depends on μ – Section III.A), mainly regarding the values of the temperature above of 423 K.

Fig. 6 illustrates the experimental I_{ON}/I_{OFF} ratios (in logarithm scale) of the different OSM and their RSM counterparts, as a function of the temperature. The I_{ON} has been obtained considering the V_{GT} equal to 4 V and V_{DS} equal to 100 mV, regarding the transistors operating in the triode region, as a closed switch. The I_{OFF} has been obtained considering the V_{GS} equal to 0 V and V_{DS} equal to 5 V, where we consider the SOI MOSFETs are operating in the cutoff region, as an open switch.

Observing Fig. 7, we can observe that the I_{ON}/I_{OFF} ratio for OSM1 and OSM2 are always higher (approximately 75% and 22% for 300 K and 492% and 42% for 573 K, where the α angles are equal to 53.1º and 90.0º, respectively) than those found in their respective RSM counterparts for all temperatures, regarding the same bias conditions.

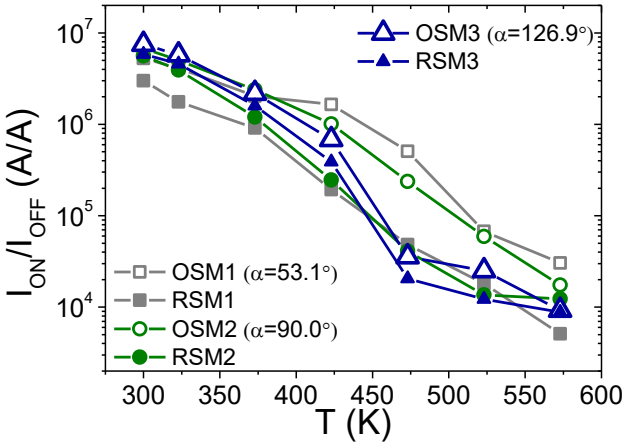

Fig.6 The I_{ON}/I_{OFF} ratio of devices as a function of the temperature.

The experimental results of I_{ON}/I_{OFF} ratios of the OSM are influenced by its higher I_{ON} values compared to their RSM counterparts (Section III.A) and, mainly, by the reduction of I_{OFF} with the increase of the temperature in comparison to the I_{OFF} values presented by their RSM counterparts, as explained in Section III.B. This is another important difference of the octagonal layout style for implementing SOI MOSFET technology in relation to the hexagonal gate geometry [14, 30], because for all temperatures considered, the OSM I_{ON}/I_{OFF} ratios are always higher to the ones found in their respective RSM counterparts.

D. On-state resistance

The on-state resistance (R_{ON}) is a very important parameter for CMOS switches applications [27]. The smaller its value, the less noise the SOI MOSFET produces. Besides, when the R_{ON} values are smaller, the MOSFETs achieve higher speeds [38].

The R_{ON} is determined when the SOI MOSFET operates in the triode region, i.e., when it operates as a closed switch and it is mathematically given by Equation (5) [33, 39]:

$$R_{ON} = \frac{1}{\left[\mu_n C_{OX1} \frac{W}{L}(V_{GS} - V_{TH})\right]} \quad (5)$$

wherein μ_n is the electron mobility and C_{OX} is the front gate oxide capacitance.

This equation is only valid when V_{DS} is much smaller than V_{GT} [20]. We can see by Equation (5) that R_{ON} is inversely proportional to the mobilities of mobile charge carriers in the channel. Therefore, when T is increasing, the mobility is reducing and consequently R_{ON} will be increasing in the channel region [2, 34, 35].

Fig. 7 presents the experimental R_{ON} of the OSM with three different α angles and their RSM counterparts as a function of T. The experimental R_{ON} values have been obtained by the ratio between the V_{DS} variation (ΔV_{DS}) in relation to the I_{DS} variation (ΔI_{DS}) in linear region of the Triode region, for V_{GT} equal to 2 V, in this case.

It is possible notice that on-state resistances of the devices increase when T increases. Besides, the OSM R_{ON} values are always significantly lower (approximately 40%, 24% and 8% for 300 K, and 59%, 25% and 5% for 573 K, regarding α angles equal to 53.1º, 90.0º and 126.9º, respectively) than those measured in their RSM counterparts. This happens due to the LCE and PAMDLE effects (high I_{DS} values - Section III.A), resulting in low values of R_{ON} and subsequently leading to higher MOSFETs I_{DS} values.

The gain provided by the octagonal layout style for MOSFET in R_{ON} are also discussed in the following references regarding numerical simulations and experimental results in room temperature [24, 25] and radiation environment [40, 41].

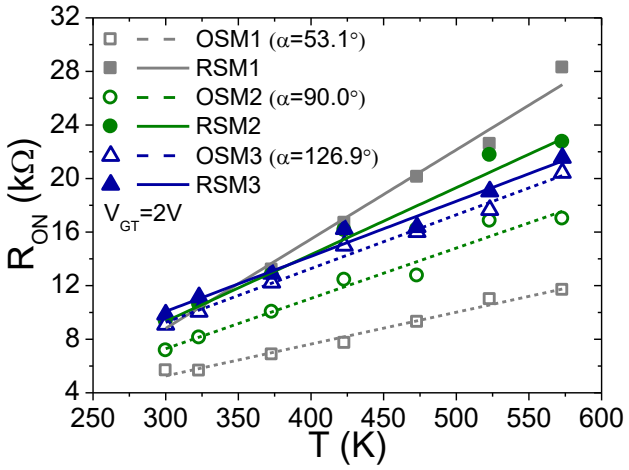

Fig. 7 The experimental R_{ON} of the OSM and their RSM counterparts as a function of T

Making an analogy with the study of reference [28], it possible to predict that the delay time constant ($\tau = R_{ON}.C_{GS}$, which C_{GS} is gate capacitance) of the OSM tends to be smaller than the one found in its RSM counterpart, regarding that both devices present the same W, and bias conditions. This can be proven by reference [28], which has shown that the gate capacitance of an ellipsoidal layout style for MOSFET (EM) is around 11% greater than the one found in its conventional MOSFET (CM) counterpart in room temperature, because its PN junctions length between the drain/source and channel regions are higher, considering both devices with the same W and bias conditions. However, the R_{ON} of the EM is 65% remarkably smaller than that those found in its CM counterpart, and therefore, the τ of the EM is significantly smaller (61%) than the one observed in its CM counterpart in room temperature [28].

Analogously, as the ellipsoidal layout style is an evolution of octagonal layout style, we can consider that the OSM will also have a gate capacitance slightly higher than the one found in its RSM counterpart, because its PN junctions length between the drain/source and channel regions are higher than the one found in its RSM counterpart (Table I). Therefore, thanks to the much smaller OSM R_{ON} values in comparison to the one observed in their RSM counterpart, the OSM delay time constant tends to be smaller than their RSM counterpart presents.

CMOS switches are extensively used in power management circuits, for example to turn off (i.e. to put in sleep mode) digital CMOS ICs [42], or in DC-DC converters [43] to generate the low IC supply voltage (e.g. 1-3 V) from the main power supply at higher voltage (typically 3-5 V). To meet efficiency objectives, such techniques require that the MOSFET switches added to the circuit must be upsized, i.e. keeping large aspect ratios (W/L) to deliver the full IC current at low voltage drop when turned on, while limiting the leakage current when turned off with a high drain-source voltage drop. Consequently, the use of MOSFETs with channel lengths (L) larger than the minimum dimension (L_{min}) allowed by the CMOS technology must be used. Therefore, the Octo SOI MOSFETs can be considered an alternative device to be used in such techniques because they present effective channel lengths (L_{eff}) larger than the L_{min}, while providing higher I_{ON} with reduced I_{OFF} when interfacing voltages of 3-5 V for high-temperature applications.

IV. Conclusion

This manuscript has reported that the octagonal layout style implemented for SOI MOSFETs technology is capable of keeping active the LCE, PAMDLE, DEPAMBBRE effects under high temperature operation (from 300 K to 573 K), consequently, notable enhancements in the main switch electrical parameters and figures of merit in comparison than those observed in their RSM counterparts, such as I_{ON}, R_{ON} and I_{ON}/I_{OFF} ratio. We have described the electrical behavior of the OSM $I_{OFF}/(W/L)$ in relation to the its SOI MOSFET counterpart, showing that the Octo layout style for SOI MOSFETs is outstandingly able to reduce the value of the SOI MOSFETs I_{OFF} and, consequently, to reduce the power consumption (ecologically-friendly solution) of the CMOS switch applications at high temperature. Moreover, as it is enormously imperative to aggregate the everlasting requirement for energetic efficiency and low cost, this layout technique does not cause any supplementary charge for the current and complex planar CMOS ICs manufacturing process.

Acknowledgements

The authors would like to thank the FAPESP (grant #2017/10718-7), CNPq (grant#308702/2016-6) and CAPES for financial support.

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