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Preface

This volume contains the papers presented at SEMINATEC 2018: XIII Workshop on Semiconductors and Micro & Nano Technology held on April 19-20, 2018 at the Centro Universitario FEI, campus Sao Bernardo do Campo, Brazil.

There were 46 submissions selected for presentation at SEMINATEC 2018, as well as the presentations of invited Distinguished Lecturers of the IEEE Electron Devices Society: Dr. Durda Misra, from New Jersey Intitute of Technology, USA, giving the talk "How Reliable the Next Generation Nanoelectronic Devices: FinFETs to Ge Devices"; Dr. Lluis Marsal, from University Rovira e Virgili, Spain, giving the talk "Polymeric Solar Cells"; Dr. Gilson Wirth, from Federal University of Rio Grande do Sul, Brazil, giving the talk "Charge Trapping Phenomena in MOSFETS: From Noise to Bias Temperature Instability. Reliability of Nanoscale Semiconductor Devices".

Additionally to these previously mentioned presentations, two national wide projects presented their results, The NAMITEC Network and The CITAR Project.

We would like to express our gratitude to the authors as well as the reviewers.

We would like to acknowledge the IEEE ED Centro Universitario FEI Student Branch Chapter, IEEE ED Universidade Estadual de Campinas Student Branch Chapter and the IEEE ED South Brazil Chapter for inviting EDS Distinguished Lecturers who enlighted the Workshop.

We also would like to express our acknowledgement to Tektronix and OKK for their sponsorship on SEMINATEC 2018.

April 19 and 20, 2018
Sao Bernardo do Campo

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Michelly de Souza
Rodrigo Trevisoli Doria
Renato Camargo Giacomini
Salvador Pinillos Gimenez
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Michelson Interferometer based All-optical NOR Logic Gates

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1. Abstract

This paper presents a study of Michelson interferometer composed of Semiconductor Optical Amplifier (SOA-MI) and symmetrically identical Fiber Bragg Grating (FBG) at the output of each of its arms, for implementation of the all-optical NOR logic gate with bit rate of 10 *Gb/s*, for high-speed optical processing and analysis of non-linear effects. The device was analysed in terms of bit error rate (BER), Q-factor, and optical spectrum, which demonstrates a high-speed gate and performance. Numerical simulation was performed on OptiSystem 15.0 software at OptiWave Corporation.

2. Introduction

A SOA is an optoelectronic device that overcomes the electronic bottleneck because of its non-linear characteristics, amplifying the signal input, providing high gain, a strong change of its refractive index [1, 2]. Its according to several modulation formats, where the cross-gain modulation (XGM) is used in this paper, in which omits the need for optoelectronic conversions, making it the best alternative for the implementation of all-optical logic functions in optical networks, being these key elements in the functionalities of nodes and make feasible the concept of signal processing, taking full advantage of the potential of optical fibers. For the detection of different optical logic gates, an optical filter at a proper wavelength and bandwidth must be selected appropriately [3].

3. Project of All-optical NOR logic gate with SOA-MI

A. Schematic of a Michelson fiber-optic interferometer

The SOA-MI scaling of the NOR gate is shown in Fig. 1. The transmitter consists of two input signals **A** and **B** through the Bit Sequence Generator with the Optical Gaussian Pulse Generator at frequency 1556 *nm* and input power 0.3 *mW*, both coupled and then combined with the Pump CW Laser at frequency 1550 *nm* and input power 0.25 *mW* through the Power Combiner 2x1, and enters the Traveling Wave SOA with injection current 0.15 *A*, which is connected to the Power Splitter 1x2 in which it has in its outputs the symmetrically identical FBGs with frequencies equal to the CW Laser. The output signals from the FBGs are again coupled with Pump Coupler Co-Propagating and pass through another Traveling Wave SOA of the same configuration. At the receiver, it performs a filter through the Gaussian Optical Filter, with a frequency of 1550 *nm* and bandwidth from 10 to 40 *GHz*, to reject interference and noise components and then converted optically into the electric form through the Optical Receiver with a cut-off frequency of 0.75 * *Bit rate Hz*, for a NRZ Pulse Generator. The output signal is viewed through the Oscilloscope Visualizer and analyzed with the Eye Diagram Analyzed.

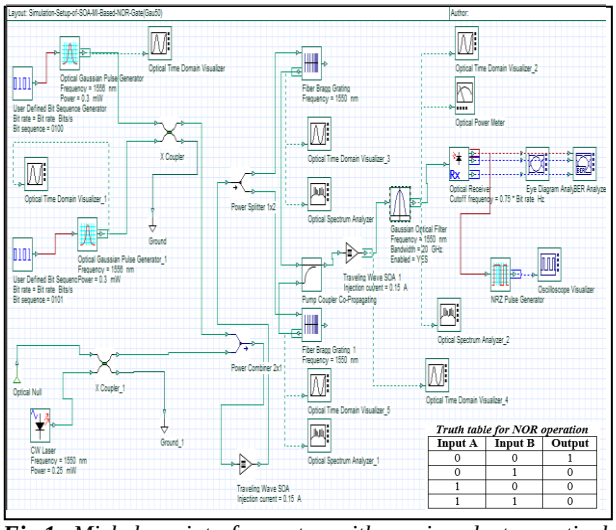

Fig.1. *Michelson interferometer with semiconductor optical amplifier for NOR Logic gate.*

4. Results and Discussions

The Table I shows the Q-factor and Min. BER of the NOR gate for different bit inputs and filter bandwidth from 10 to 40 *GHz*. The Table II shows the different bit numbers 4, 8 and 16-bits and their respective outputs. The Fig. 2 shows the results of the Oscilloscope Visualizer for the 4-bits sequence of 40 *GHz*, since it presented the best results for the Q-factor and Min. BER between the simulations. It was observed that the variation of the filter bandwidth did not change the result of the logic gate at the output of the optical signal.

Table I. *Analysis of the results for different bit inputs and filter bandwidth from 10 to 40 GHz.*

Number of Bit	Parameters					
	10 GHz		20 GHz		40 GHz	
	Max. Q-Factor	Min. BER	Max. Q-Factor	Min. BER	Max. Q-Factor	Min. BER
4-bits	3.02524	$7.973x10^{-4}$	3.399	$2.858x10^{-4}$	3.55147	$1.697x10^{-4}$
8-bits	2.77484	$2.736x10^{-3}$	2.51273	$5.989x10^{-3}$	0	1
16-bits	2.33527	$9.692x10^{-3}$	2.68967	$3.375x10^{-3}$	2.80582	$2.315\ x10^{-3}$

Table II. *The different number of bit for NOR operation.*

Signal	Number of Bit		
	4-bits	8-bits	16-bits
Input A	0100	01011010	0100001111000011
Input B	0101	00110000	0101110111011100
NOR	1010	10000101	1010000000100000
NOR Gate Symbol	A B out		

A. The result for 4-bits input signal

The result (1010) shown in Fig. 2 is an NOR gate realized using an SOA-MI, of the 4-bits for ports **A** (0100) and **B** (0101) with bit rate 10 *Gb/s*. The Fig. 3 presents the result for 16-bits sequence (0100001111000011), having as inputs **A** (0101110111011100) and **B** (1010000000100000).

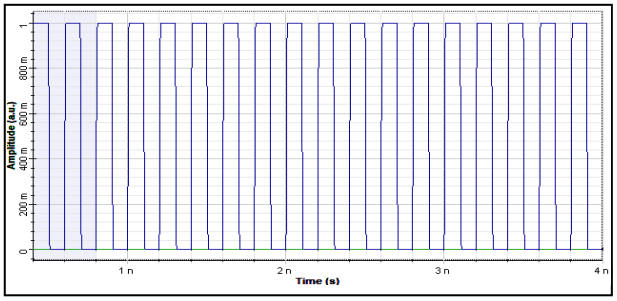

Fig.2. *Simulated result output of signal at NOR logic gate (1010) of 4-bits for 40 GHz.*

B. The result for 16-bits input signal

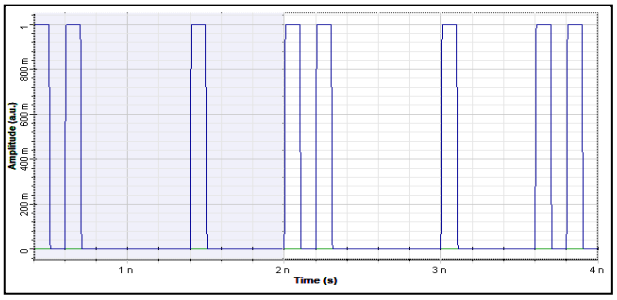

Fig.3. *Simulated result output of signal at NOR logic gate (1010000000100000) of 16-bits for 40 GHz.*

The Eye Diagram shown in Fig. 4 refers to the 4-bits result with 40 GHz filter bandwidth.

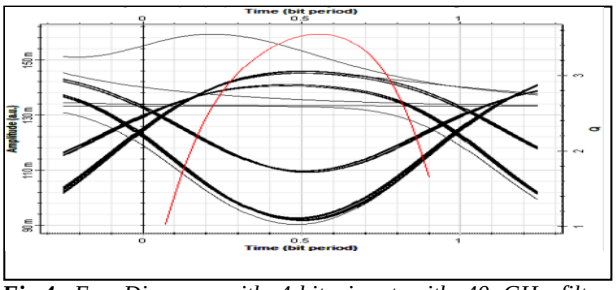

Fig.4. *Eye Diagram with 4-bits input with 40 GHz filter bandwidth.*

5. Conclusions

The results showed the efficiency of the use of MI-based SOAs for the implementation of the all-optical NOR logic gate in a simple and compact way, using different numbers of bits (4, 8 and 16) of the input signals **A** and **B**, and filter bandwidth (10 to 40 *GHz*) at a bit rate of 10 *Gb/s*. Other logical gates can be analyzed with the implementation of SOA-MI, and also use of greater number of bits for the input.

Acknowledgments

The Optiwave developer of the OptiSystem simulator and the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (CAPES).

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Influence of UV Light on (BE) SOI pMOSFET

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Abstract

This paper presents for the first time the influence of ultraviolet (UV) light on BE SOI pMOSFET at different operational regions. The best bias operation region is analyzed and it is observed that the BE SOI pMOSFET is more sensible to UV light when the conduction at front interface is more relevant.

1. Introduction

The BE (Back Enhanced) SOI MOSFET is a new device developed and fabricated at Laboratório de Sistemas Integráveis (LSI) from the University of São Paulo (USP) [1,2]. Its main advantages are the reconfigurable operation (can work like pMOS or nMOS) and simple planar fabrication technology, without necessity of any intentional doping steps. It is a kind of undoped junctionless MOSFET but with very different conduction mechanism. In total only three photolithography masks are required [1,3,4].

2. Device Characteristics

The BE SOI pMOSFET was fabricated at Laboaratório de Sistemas Integráveis from the University of São Paulo. It was built on a SOI wafer with buried oxide thicknesses of 200nm and natural Boron concentration of 10^{15} atoms/cm^3. The BE SOI features aluminum gate electrodes and silicon film and gate oxide thickness of 10nm each.

Nickel is used as source/drain electrodes. This metal was used to provide more equilibrium between Schottky barriers of holes and electrons, thus improving the revertible behavior [3].

The device studied in this paper had a gate length and width of 100µm. Fig. 1 [3] illustrates the device profile along with its real dimensions (not to scale).

3. Device Operation Regions

Considering that the BE SOI does not have any intentional doping steps, a back gate (V_{GB}) bias is required to induce a layer of charges on the back interface, thus electrically connecting the source and drain. This is the principle of reconfigurability. If the back gate V_{GB} is positive enough, electrons are induced at the back interface and the device will work as an n-type transistor. Otherwise, if V_{GB} is negative enough, holes are created and a p-type operation is achieved [3,4].

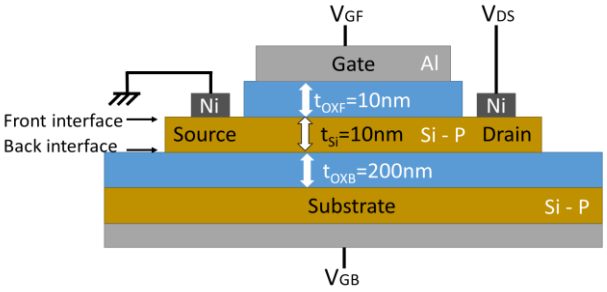

Fig.1. *BE SOI MOSFET profile (not to scale) [3].*

After the formation of the carrier layer, applying a voltage between the drain and source (V_{DS}) allows a current to flow between those terminals. This current can be modulated by a bias on the front gate (V_{GF}). On n-type operation, for more negative values of V_{GF} (for more positive on p-type) lower is the drain current [4]. On the other hand, a large enough V_{GF} can extinguish the carrier layer (off state) [1].

Fig. 2 shows I_{DS} x V_{GF} curves for both p- and n-type device operation [4]. One can notice that the current tends to be constant at certain level for higher $|V_{GS}|$ bias. This characteristic is analyzed in the following paragraph for a p-type device, but it is analogous for n-type ones.

It is possible to split the I_{DS} x V_{GF} curve in three operational regions as shown in Fig. 3 [3]. In the region A, the front gate bias depletes all channel region and the device is in OFF state. In the region B, a more negative

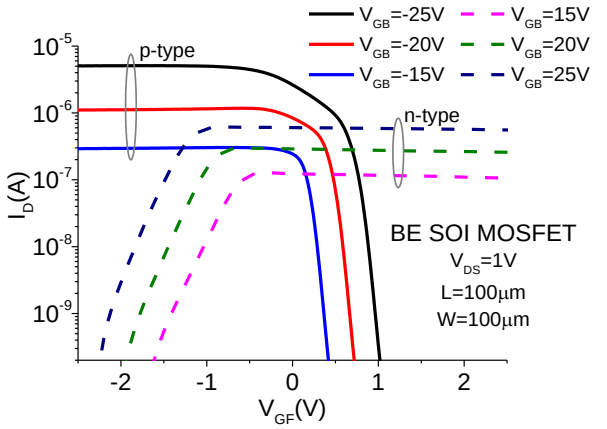

Fig.2. *BE SOI MOSFET characteristics for both p-type (V_{GB}<0) and n-type (V_{GB}>0) operations. [4].*

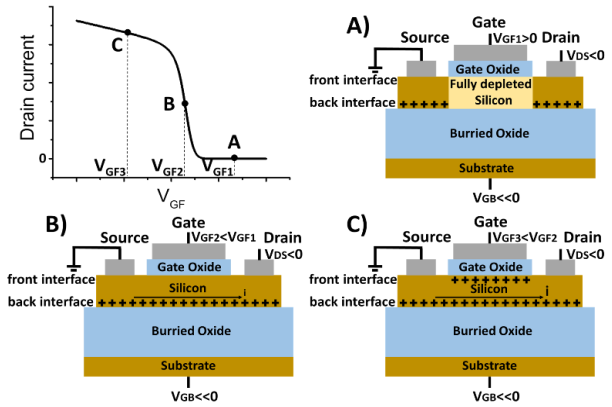

Fig.3. *Drain current as a function of the front gate voltage V_{GF}. A) Device profile in the off-state for $V_{GF1}>V_{TH}$. B) Device profile in the on-state for $V_{GF2}<V_{GF1}$. C) Device profile in the on-state for $V_{GF3}<V_{GF2}$ [3].*

V_{GF} reduces the depletion region, therefore increasing the drain current. Lastly, in region C there is no more depletion and decrementing the value of V_{GF} only contributes to the accumulation of holes under the front gate (front interface). This layer of charges does not contribute much for increasing the drain current because, in the front interface, there is a region of high resistivity between the gate and source/drain electrodes. Hence, the current flows mostly through the back interface and it tends to saturate [3].

4. Optical Sensitivity

The device's optical sensitivity was also experimentally measured inside the UVA spectrum (λ = 315~400 nm). The setup consisted of 16 LEDs (Ø = 5 mm) irradiating UV light at 2.5 cm from the wafer. The wavelength of peak intensity is about 400 nm and the current flowing through each one was 20 mA.

Fig. 4 shows two I_{DS} x V_{GF} curves of the same device operating as a BE SOI pMOSFET, one with UV irradiation another with the UV turned OFF. One can notice a much higher difference between both curves in the region C (V_{GF} << 0) than in other regions. For better visualization, the difference between these currents (ΔI_{DS}) was also plotted. The ΔI_{DS} obtained in the region C was about 30 nA for V_{GF} between -2.5 and -3.0V.

Based on these results, it is observed that the BE SOI pMOSFET is almost insensible when the current flows at the back interface. A major influence is observed in the C region, where carriers are induced to the front interface. The electron-hole pairs generated by the UV light can reduce the resistance on the gap between the gate and source/drain electrodes. The result is a higher value of the saturated drain current. Under this bias condition, the BE SOI pMOSFET can be used as a UV light sensor.

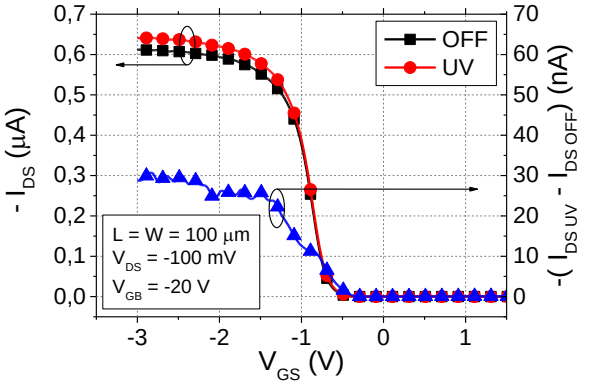

Fig.4. *Experimental BE SOI pMOSFET transference characteristics with UV radiation (circles) and without any luminous incidence (squares). The difference between both curves are also shown (triangles).*

5. Conclusion

This paper presents for the first time the influence of ultraviolet (UV) light on BE SOI pMOSFET at different operational regions. The experiment results show that the optical generation is more relevant on the drain current flowing through the front interface (region C) than in the case where I_{DS} only flows at the back interface (region B). In region C condition, the BE SOI pMOSFET can be used as a UV light sensor.

Acknowledgments

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Optical characterization of graded porous silicon by XRR, GISAXS and SLIM

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1. Abstract

Porous silicon (PS) monolayer with graded refractive index was investigated by X-ray reflectance (XRR), grazing incidence small X-ray spectroscopy (GISAXS), and spectroscopy by liquid infiltration method (SLIM) to compute the thickness, effective refractive index, the porosity, and pore size. The results point out that the thickness of this layer is about 6578 nm, whereas its porosity ranges from about 70- 81% in depth. GISAXS reveals that the system is composed by a set of spherical pores with radius between 3.0 and 4.4 nm and cylindrical ones with length of about 55-102 nm.

2. Introduction

Porous silicon is an extensively investigated material because of its singular physical and chemical properties that makes it an excellent material for photonic and sensor applications, for instance [1,2]. PS monolayers are commonly assumed be homogeneous in depth, but different research groups have demonstrated that depending on the electrolyte features and pores size a porosity gradient can be appear because difficulties in electrolyte diffusion toward the deeper regions, as well as due to the fluoride species consumption [3]. The importance of this gradient becomes critical in one-dimensional photonic crystal structures because this gradient yields the formation of a gradient of the effective refractive index of its individual layers[2]. In this sense, here we report the optical characterization graded PS monolayer by using X-ray reflectometry, GISAXS and SLIM.

3. Experimental procedure

A PS monolayer was made by anodizing a heavily p-type silicon (100) with resistivity of about 0.001 Ωcm into electrolyte composed by HF: ethanol (1:3) and applying 15 mA/cm^2 of current density during 400 s. The graded porosity was formed by keeping the mesoporous structure (meso-PS) during the electrolyte for additional 30 minutes for chemical dissolution. For its characterization, XRR and GISAXS were employed, in addition to the SLIM which was made with the help of a Black Comet Spectroradiometer within spectral range of 350-1100 nm. For the GISAXS experiment, the sample-detector distance was about 30 cm, impinging the X-ray beam at about 0.20° in order to improve the intensity. For the SLIM experience, the pores were filled by methanol (n = 1.327) and the reflectance spectra were employed to compute the thickness, and porosity.

4. Results and discussions

The reflectance spectra of the single graded mono layer immersed in air and methanol are observed in Fig. 1. In this picture is clear the graded nature of this sample because the absence of regularity in the interference fringes size. In addition, the spectrum from the meso-PS immersed in methanol appears red-shifted in relation to that measured from the air medium. It happens because the effective refractive index variation owing to the presence of methanol within the pores. From these spectra, the porosity (≈ 70 %) and thickness (≈ 6578 nm) was estimated by solving (1) and (2) [4].

$$P = 1 - \frac{\left[\left(OT_{air}/d\right)^2 - n_{air}^2\right]\left[2\left(OT_{air}/d\right)^2 - n_{Si}^2\right]}{\left[3\left(OT_{air}/d\right)^2\right]\left[n_{Si}^2 - n_{air}^2\right]} \quad (1)$$

$$P = 1 - \frac{\left[\left(OT_{meth}/d\right)^2 - n_{meth}^2\right]\left[2\left(OT_{meth}/d\right)^2 - n_{Si}^2\right]}{\left[3\left(OT_{meth}/d\right)^2\right]\left[n_{Si}^2 - n_{meth}^2\right]} \quad (2)$$

Where $OT_{air} = n_{air}d$ and $OT_{meth} = n_{meth}d$ are the optical thickness of the layer in air and methanol, respectively, and d the PS thickness.

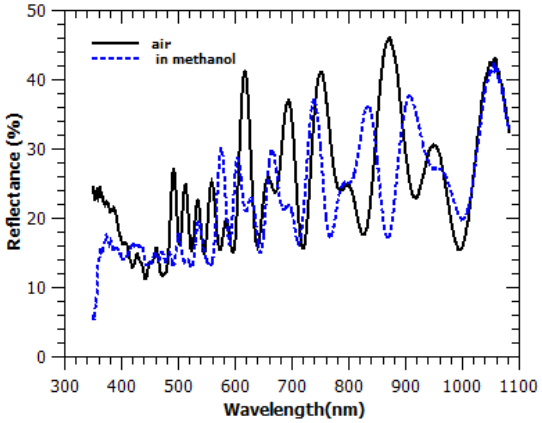

Fig.1. *Reflectance spectra from mesoporous sample immersed within air (solid line) and methanol (dashed line).*

In Fig. 2 is depicted the XRR spectrum from the meso-PS structure here investigated. The typical interference fringes expected for a single layer is lack because the meso-PS thickness is about 6578 nm, in addition to the larger roughness of the air/meso-PS and meso-PS/Silicon interfaces, being them about 8.5 and 1.0 nm, respectively, as revealed by Parrat32 code. Unfortunately, XRR was unable for computing the thickness because the interference fringes lack, but the

presence of two peaks linked to the critical scattering-vector q_z for silicon ($q_{c,si}$ = 0.0305 A^{-1}) and meso-PS ($q_{c,PS}$ = 0.0305 A^{-1}) is clear, from which the porosity was computed to be c.a 76% by (3)

$$p(\%) = 1 - \frac{q_{c,PS}^2}{q_{c,si}^2} \quad (3)$$

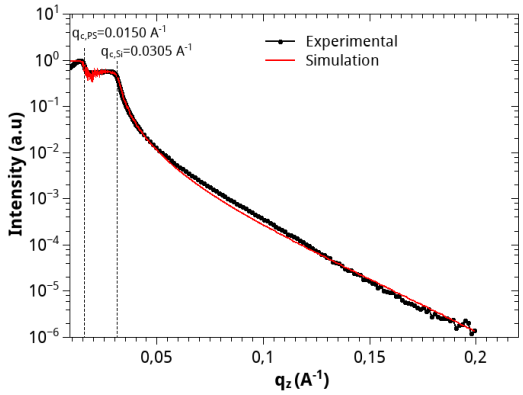

Fig.2. *XRR spectrum from meso-PS irradiated at incidence angle equal to 0.20°*

In Fig. 3 are depicted the one-dimensional GISAXS (inset) extracted from the two-dimensional GISAXS (not shown here) and the Kratky plot. These curves were fitted using the generalized Ostern-Zernike relationship given by (4) [5]

$$I = I_o \sum_{k=1}^{4} \frac{f_k}{1 + (\varepsilon_k q_y)^{n_k}} \quad (4)$$

Where ε_k and I_o are the correlation length and the incident intensity, respectively, while f_k is a fitting parameter. n_k represents the geometrical features of the objects [5]

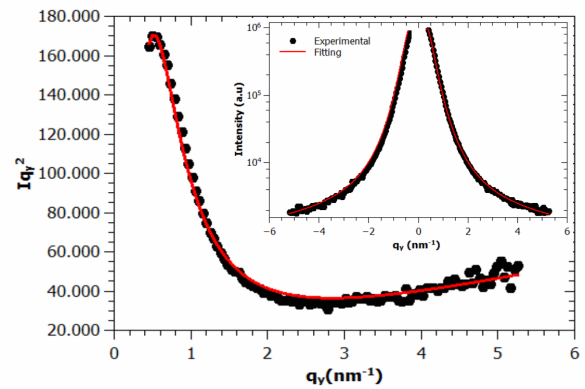

Fig.3. *Kraky plot taken from one-dimensional GISAXS (inset) at q_z = 0.72 nm.*

The curves in Fig. 3 were reasonable fitted regarding the porous layer composed by two spherical ($n_k \approx 4$) and two cylindrical ($n_k \approx 1$) pores with different geometrical dimensions, as is summarized in Table 1. Porosity was estimated to be around of 81% by computing the invariant Q and using the electron density of silicon, ρ_{Si} = 0.6981 cm^2 in (5) [5]

$$Q = \int I q_y^2 dq_y = 2\pi\rho^2 p(1-p) \quad (5)$$

The apparent divergence between the values obtained by XRR and GISAXS can be explained in the sense that porosity from XRR represents the effective value of the entire structure, whereas that obtained from GISAXS represents the value at $q_z \approx 0.72$ nm^{-1}, which corresponds to the superficial region. In the case of the low value of porosity (≈ 70%) by SLIM, it could be due to the not complete filled of the pores owing to the surface tension effects.

Table I. *Geometrical features of the pores within the mesoporous layer.*

f_k	n_k	ε (nm)	R_g (nm)	R (nm)	H (nm)
18,0	3,98	2,6	3,43	4,42	-
23,8	3,95	1,8	2,38	3,07	-
3,0	1,02	15,0	29,60	41,85	102,38
0,5	1,00	8,0	16,00	22,63	55,29

4. Conclusions

Graded PS monolayer was fabricated and characterized by XRR, GISAXS and SLIM. It was found that porosity varies in depth due to the chemical dissolution effect, reason by which the reflectance spectra becomes far from that observed in single monolayers. In addition, XRR reveals that the roughness interface can be larger as 8.5 nm reason by which no interference fringes is observed. The porosity obtained by these means diverges from each other, varying from 70% to 81% in depth and the porous structure can be modeled as composed by spheres and cylinders.

Acknowledgments

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Electrical characterization of MPS/SiO_2/PANI heterostructure for sensors

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1. Abstract

Macroporous silicon (MPS) layer was passivated by chemical oxidation and then polyaniline (PANI) was deposited chemically within the porous structure to fabricate a heterostructure to be used as sensor. The structural characterization of this device by scanning electron microscopy (SEM) reveals the effectiveness of the chemical method for PANI deposition in oxidized porous matrix. The analysis by ATR-FTIR shows that PANI was deposited in its most conductive phase, forming a well-defined replica of the porous structure. The electrical characterization shows that conductivity along the sample surface direction is basically dominated by PANI, whereas between the PANI and substrate is determined by silicon.

2. Introduction

Porous silicon (PS) is a widely-investigated material because of its singular physical and chemical properties that makes this material suitable for applications such as light emitting diodes [1]. Undoubtedly, one of the most promising applications of PS is in the sensor field because of its larger effective surface in which a larger number of sensing species can be attached [2]. For sensors, it is desirable that both optical and electrical responses be only due to the presence of the analyte and not due to the transducer degradation. In this sense, different strategies have been employed to avoid the PS/analyte interaction, such as the passivation by silicon oxide (SiO_2) [3], but the optimal performance of these sensors depends on the functionalization because it improves its selectivity and sensitivity [2,4]. In this sense, polyaniline (PANI) seem to be excellent for this task because of its highly stable chemical properties even under room conditions [5]. Here, it is reported the structural and electrical characterization of MPS/SiO_2/PANI heterostructure for sensor applications.

3. Experimental procedure

A set of p-type crystalline Si (100) with $\rho \approx 10\ \Omega$.cm were cleaned following the CMOS procedure, and then deposited 0.5 mm of aluminum on its backside; after, they were sintered at 500°C in N_2 environment. For pore formation, they were anodized in HF:DMF (1:9) by applying 10 mA/cm^2 of current density during 5.0 min. In the next step, they were electrochemically oxidized immersing the samples into H_2SO_4:H_2O (1:5) and then applying 10 mA/cm^2 of current density during 20 min. Finally, PANI was deposited chemically in the oxidized MPS (OMPS) by immersion in 1 M HCl, 1M aniline and 0.25 M of $(HN_4)_2S_2O_8$ during 24 hours in darkness.

The structural characterization was made by the scanning electron microscopy (SEM), whereas for the electrical one the current-voltage and impedance response were measured between two points along the device surface (superficial) and between the surface and the substrate (transverse). The contacts were made by two silver spots with about 5 mm of diameter on the PANI, while the contact at the substrate was made by the Al layer. In addition, an attenuated total reflectance infrared spectroscopy (ATR-FTIR) Spectrum 100 Perkin Elmer equipment was employed to investigate the PANI presence within the porous structure.

4. Results and discussions

Fig. 1a and 1b show the cross-section and top-view SEM images, respectively, from the MPS/SiO_2/PANI heterostructure, in which the presence of PANI onto its surface is noticeable. In addition, Fig. 1b shows that the PANI thickness inside the pores is about 38 nm and was placed on SiO_2 intermediate layer with thickness c.a 20 nm. This layer is stressed by arrows because difficulties to be visualized as consequence of the poor mass density contrast between silicon and SiO_2 (ρ_{Si} = 2.33 g/cm^3 and ρ_{SiO2} = 2.20 g/cm^3).

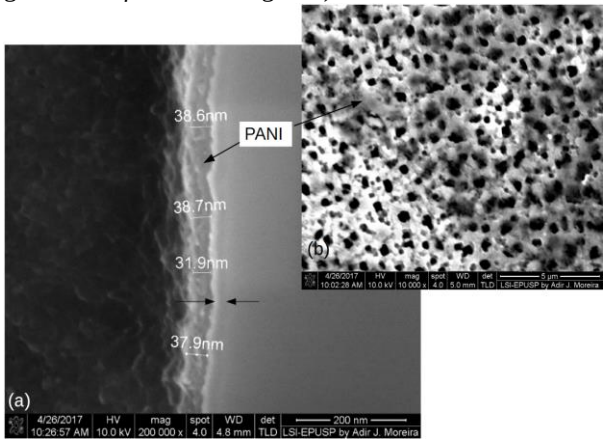

Fig.1. *(a) Cross-section and (b) top-view SEM images from PANI/SiO2/PS heterostructure.*

The FTIR spectra from OMPS and MPS/SiO_2/PANI structures are shown in Fig. 2. There, the peaks at 664, 800, 878, 1036, and 1056 cm^{-1} correspond to the Si-O-Si bonds and evidences the SiO_2 growth in the structure [6]. For the MPS/SiO_2/PANI, the peaks at 1502 and 1588

cm^{-1}, along with that at 1238 cm^{-1} belong to the C-C and C-N stretching bonds of the benzenoid ring, while the peaks at 1298 cm^{-1} and those located at 1303, 1334, 1378 cm^{-1} correspond to the C-C and C-N stretching bonds of the quinoid rings. In the case of the peak at 1146 cm^{-1}, it is typical in PANI deposited via HCl solution. The peaks at 1118, 1168, 1213, 1303 and 1378 cm^{-1} it is attributed to the C-H, C-C or N-H bonds [6].

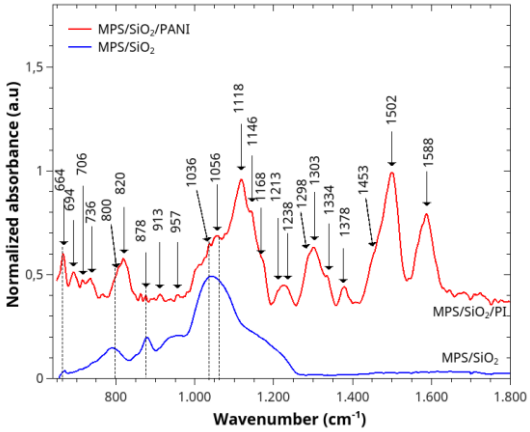

Fig.2. *ATR-FTIR spectra from MPS/SiO$_2$/PANI and OMPS.*

The Fig. 3a shows the current-potential curves measured from the lateral and transverse direction with differences each other. In the case of the lateral direction, the curve appears almost symmetrical claiming the predominating contribution of PANI for charge transfer, but the lower current intensity shows the lager resistance due to the porous structure. This result is also observed through the bigger semicircle observed in Fig.3b. For the transverse direction, the non-symmetrical current-potential curve (Fig. 3a) is typically observed in metal/semiconductor junction and behaves as a Schottky diode [1]. Unlike that observed in the superficial direction, it appears with larger current intensity due to the low electrical resistance, which is confirmed by the small semicircle in Nyquist plot (Fig. 3b).

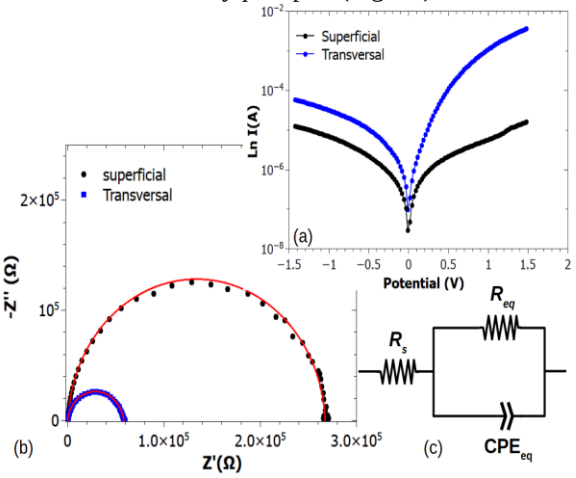

Fig.3. *(a) Current-potential curve, (b) Nyquist plot, and (c) equivalent electrical circuit for the MPS/SiO$_2$/PANI.*

Although the system is composed by MPS, PANI and SiO_2, the presence of a semicircle feature in the Nyquist plot suggest that the system can be regarded as composed for a single effective layer. Therefore, the corresponding equivalent electrical circuit of the MPS/SiO_2/PANI can be observed in Fig. 3c, changing the capacitance by a constant phase element (CPE). The impedance for it was defined by (1):

$$Z_{CPE} = \frac{1}{P\omega^n}\exp\left(-\frac{\pi}{2}i\right) \quad (1)$$

Where P is a constant equivalent to the capacitance and ω the frequency. Using this approach, the results describing the heterostructure is summarized in Table 1.

Table I. *Electrical parameter extracted by fitting the Nyquist curves for the MPS/SiO$_2$/PANI heterostructure.*

direction	R_s (Ω)	R_{eq} (kΩ)	n	P (nF)
Superficial	248.56	267.71	0.966	1.04
Transverse	33.78	57.84	0.935	7.22

4. Conclusions

Electrical properties of MPS/SiO_2/PANI heterostructure were investigated. It was shown that chemical route is suitable for PANI deposition inside the pores of OMPS, as revealed by the ATR-FTIR, forming a thin layer of about 32 nm. The current-voltage curves from superficial and transverse direction are different each other and reveals that conductivity along the surface is predominantly determined by PANI, whereas along the transverse one is dominated by silicon. The Nyquist curve shows that the system can be regarded as composed only by one effective layer.

Acknowledgments

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Comparative Study on the Performance of Silicon and III-V Nanowire Gate-All-Around Field-Effect Transistors for Different Gate Oxides

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1. Abstract

This paper presents a comparative study between silicon and III-V nanowire gate-all-around field-effect transistors (NW-GAA-FET), performed on COMSOL Multiphysics. For this purpose, we calibrated, first, the simulated results with the experimental data of a silicon nanowire manufactured by Yang et al. [1]. Posteriorly, we extend the simulation analysis to III-V semiconductor materials, such as GaSb, GaN, GaAs and InP, as well as considering distinct gate oxides: SiO_2, Si_3N_4 and HfO_2. Finally, we performed the comparative analysis on the electrical performance of the FETs based on the extraction of the drain-induced barrier lowering (DIBL), subthreshold slope (SS) and the I_{on}/I_{off} ratio from the simulated I-V curves.

2. Introduction

Devices based on semiconductor nanowire have been attracted a great deal of interest for electronic and photonic applications, especially the silicon and III-V NW-GAA-FET [1]-[5].

Advances in manufacturing techniques in the last few years have allowed improved size control, with a higher flexibility in sample processing, more freedom for bandgap engineering, and many other features [6].

For instance, in 2008 Yang et al. [1] reported a Si-NW-GAA-FET on bulk silicon wafer exhibiting excellent transistor features at room temperature. Song et al. [7] reported, in 2014, the manufacturing of an III-V junctionless GaAs-NW-GAA-FET, aiming low power applications.

Both quoted devices [6-7] employ SiO_2 as oxide material, adjoined at the gate contact. However, more recently, gate oxides with high-k values have been reported on technical literature [8], in order to enhance the FET electrical features.

In this context, we propose, in this work, a comparative study on the electrical performance of silicon and III-V (InP, GaSb, GaN and GaAs) NW-GAA-FET constituting distinct gate oxides (SiO_2, Si_3N_4 and HfO_2). Numerical simulations are performed on COMSOL Multiphysics, supported by experimental data [1]. As a result, we verified that the III-V transistors exhibit a better performance than the silicon ones, as well as the replacement of SiO_2 for higher-k oxides leads to a graceful improvement on the electric merit figures: a maximum reduction of 66% for DIBL (GaSb-NW), subthreshold-slope values approaching to the theoretical limit (GaAs-NW) and a maximum increasement of two orders of magnitudes for I_{on}/I_{off} (InP-NW).

3. Device Structure and Validation

A schematic illustration of the both geometric and electrical structure of the device used to validate the simulated results with the experimental data reported by Yang et al. [1] is depicted on Figure 1. The Si-GAA-NW-FET is constituted by a silicon nanowire with a gate contact built all around the channel (GAA), while the drain and source contacts are located in the device extremities.

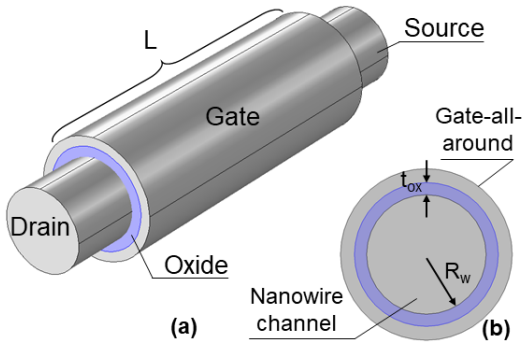

Fig.1. *(a) Schematic representation of simulated Si-GAA-NW-FET. (b) Si-GAA-NW-FET cross section.*

We used the COMSOL Multiphysics version 5.3a for the simulations of NW-GAA-FETs. In all numerical evaluations, we set the values of the following parameters in concordance to those reported on [1]: temperature (293.15 K); acceptors dopant concentration (10^{14} cm^{-3}); donors dopant concentration (10^{18} cm^{-3}); gate oxide thickness (t_{ox} = 5 nm); gate contact length (L = 100 nm) and nanowire radius (R_w = 12.5 nm).

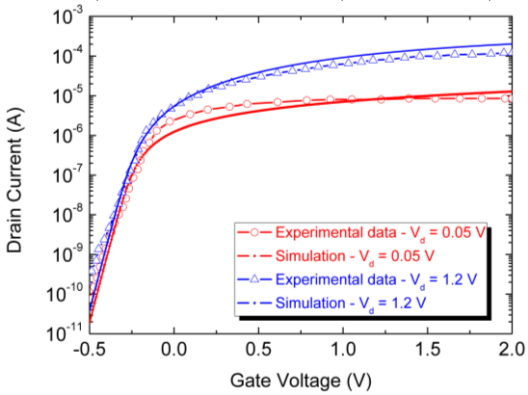

Fig.2. *I-V curves comparison between the results produced by the simulations and the experimental data reported on [1].*

In order to verify the consistency between the simulated curves and experimental data [1], we performed the calibration of the drain current as a function of the gate voltage for values of drain voltage (V_D) of 50 mV and 1.2 V. The contrasted curves are show on Figure 2.

An excellent agreement was obtained between the simulated curves and the experimental data. Thus, we have considerate that Si-NW-GAA-FET setup configured on the simulator was properly adjusted, allowing to extend our analysis regarding both distinct semiconductor channels and oxide gate materials.

4. Results

After validating the simulator, we have extracted the DIBL, SS and I_{on}/I_{off} parameters from the I-V curves, as conducted on ref. [9]. Then, we expand our numerical analysis to distinct gate oxides (SiO_2, Si_3N_4 and HfO_2), as well as by the replacement of silicon nanowire to GaSb, GaN, GaAs and InP. The results of these studies are summarized on Table I.

Table I. *Parameters extracted from the simulated I-V curves of the several devices with different gate oxide values.*

NW channel	Gate Oxide – SiO_2 (k = 3,9)			
	DIBL (mV/V)	SS (mV/dec)	I_{on}/I_{off} V_d = 50 mV	I_{on}/I_{off} V_d = 1.2 V
Si	15.8	64.2	1.1×10^7	2.0×10^8
GaSb	22.9	62.9	9.5×10^7	1.7×10^9
GaN	15.5	62.2	3.9×10^7	6.7×10^8
GaAs	18.3	61.9	3.0×10^8	5.4×10^9
InP	17.6	62.0	1.3×10^6	1.1×10^7
NW channel	Gate Oxide – Si_3N_4 (k = 7,5)			
	DIBL (mV/V)	SS (mV/dec)	I_{on}/I_{off} V_d = 50 mV	I_{on}/I_{off} V_d = 1.2 V
Si	10.8	62.1	2.2×10^7	3.5×10^8
GaSb	12.4	60.9	1.3×10^8	2.3×10^9
GaN	7.2	60.7	6.1×10^7	6.8×10^8
GaAs	10.9	60.3	3.8×10^8	6.6×10^9
InP	10.3	60.4	2.8×10^6	4.6×10^8
NW channel	Gate Oxide – HfO_2 (k = 22)			
	DIBL (mV/V)	SS (mV/dec)	I_{on}/I_{off} V_d = 50 mV	I_{on}/I_{off} V_d = 1.2 V
Si	7.8	60.9	4.6×10^7	5.2×10^8
GaSb	7.8	59.7	2.2×10^8	4.1×10^9
GaN	7.1	60.1	9.5×10^7	1.6×10^9
GaAs	7.2	59.4	8.4×10^8	1.5×10^{10}
InP	7.1	59.5	6.6×10^7	1.1×10^9

Analyzing the values presented on Table I, the exchange of SiO_2 gate oxide for Si_3N_4 or HfO_2 resulted on the DIBL enhancement for all transistors. A significant reduction of this electrical parameter was registered for the III-V materials, specifically for the GaSb (66%).

For higher values of gate oxide permittivity (dielectric constant), the SS decrease for all devices, especially for GaAs-NW-GAA-FET, which value of 59.4 mV/dec closely approaches to the theoretical limit of 58.2 mV/dec (@ T = 293.15 K).

Finally, the I_{on}/I_{off} ratio values increase for all the devices, when using the oxide gate with high-k (HfO_2). For instance, the InP-NW-GAA-FET exhibited an improvement in the I_{on}/I_{off} ratio of about 5,000% and 10,000%, respectively, for V_D values of 50 mV and 1.2 V.

Thus, we conclude that the exchanging the channel of the Si for another III-V materials or replacing the gate oxide SiO_2 for HfO_2 leads to a significant improvement in the operating parameters of the transistors. Although the silicon being one of the most abundant semiconductor material found on Earth, its replacement on the transistor manufacturing would comply with some specific electrical design features.

5. Conclusions

In this paper, we developed a simulated Si-NW-GAA-FET and then compared satisfactorily the results with the device made by Yang et al. [1]. Thereafter, we extended the simulation replacing the Si channel for different III-V materials, such as GaSb, GaN, GaAs and InP, as well as different gate oxides, SiO_2, Si_3N_4 and HfO_2. With the results, it was possible to verify the improvement on the performance of the transistors, with the substitution of Si by other semiconductors III-V, and with the use of gate oxide with higher-k values [8].

Acknowledgments

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Behaviour of the Output Conductance Due to Self-Heating Effect in SOI UTB and UTBB Transistors

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1. Abstract

The main focus of this paper is to study the behaviour of the output conductance due to self-heating in advanced Ultra-Thin Body (UTB) and Ultra-Thin Body and BOX (UTBB) SOI MOSFETs through 2D numeric AC simulations. In RF applications, the output conductance (g_D) constitutes an important characteristic to count in device design, and it is well known that SOI MOS transistors suffer from self-heating effect that degrades the output characteristics of the device including the g_D. In this work, it could be observed that the variation of g_D is more accentuated in devices with thicker buried oxide layer, which suffer from a severe self-heating.

Keywords- SOI, Self-Heating, UTB, UTBB, Output Conductance.

2. Introduction

To keep the demand for processing and performance, an even more large-scale integration of MOS device is necessary and, to reach this level of miniaturization, devices architecture becomes an important feature. With this miniaturization, undesirable effects occur like the influence of the source/drain junctions depletion on the channel charges, degrading their output characteristics. These effects are so-called Short Channel Effects (SCEs) [1]. SOI technology (Silicon-on-Insulator) [2] constitutes an alternative to continue the miniaturization process with reduced undesirable effects, where an insulating layer (Buried Oxide – BOX) has been added to separates the active region, where the devices are fabricated, from the substrate. Due to the worse thermal conductivity of the insulating material, usually SiO_2, the heat dissipation becomes more difficult, causing the self-heating (SHE) of the device. The temperature increase provokes a reduction in the electrons mobility that leads to the degradation of its output characteristics.

In order to improve devices performance, new architectures of SOI structures have been proposed. One of them is the UTB [3] (Ultra-Thin Body) MOSFET, which presents an ultra-thin silicon layer on the channel region. The reduction on the silicon layer thickness (t_{Si}) promotes a better capacitive coupling of the structure, leading to a better performance against the SCEs [3]. However, the smaller silicon area comes with the penalty of degrading the thermal conductivity of the device, making the UTB suffering from a more intense SHE.

More recently, a new SOI architecture called Ultra-Thin Body and BOX (UTBB) [4] MOS transistor was developed. Besides a thinner t_{Si}, this structure also presents ultra-thin buried silicon oxide layer (t_{box}). Due to the thinner BOX, this device enables the application of active substrate bias, i.e. the substrate can work as a second gate, improving the device performance and making it a strong candidate for low power and RF applications with performance similar to multi-gate transistors [5]. It has been recently shown that the t_{box} reduction has led to a better thermal dissipation, reducing SHE [6]. For that reason, this work aims at evaluating the AC behaviour of UTB and UTBB devices, specifically the g_D, through AC simulations, aiming at RF applications.

3. Devices Characteristics

The simulated structures present gate length (L) of 25 nm, t_{Si} = 7 nm and gate oxide thickness of 2 nm. The buried oxide thickness has been varied between10, 20, 40, 60, 80, 100, 200 and 400 nm, the source and drain regions are doped with arsenic with a concentration of $5x10^{20}$ cm^{-3}. All the simulations have been performed using Sentaurus TCAD [7] and models accounting for the carriers generation and recombination, mobility dependence on vertical and longitudinal electric fields and bandgap narrowing have been considered. For taking into account the self-heating effect, the hydrodynamic transport model has been set on, which also considers the impact ionization effect in the output characteristics. To obtain a near real device, simulations have been calibrated according to the experimental results presented in [8] and [9].

3. Applied Methodology and Results

AC simulations have been performed and the output conductance (g_D) was extracted for each device in a wide frequency range from 4 KHz up to 4 GHz ($V_{GS} = V_{TH}$ + 0.8 V and V_{DS} = 1 V).

Fig 1. presents the g_D behavior as a function of the frequency and, one can observe that there are transitions along the curve. According to [9], due to the thinner BOX, the first g_D transition is related to the substrate effect where the minority carriers do not respond to the AC signal, the second transition is related to the removal of the dynamic SHE and the third g_D transition is related to the substrate effect where the majority carriers in the

substrate do not respond to the AC signal. The main focus of this work is on the SHE effects, and so, the second g_D transition has been evaluated.

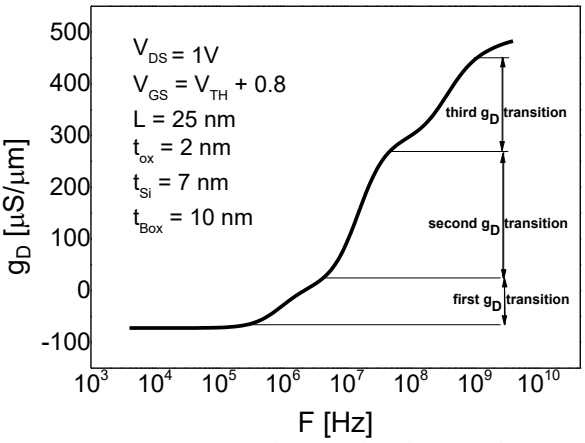

Fig.1. *Output Conduction as a function of the frequency for a UTBB device with L = 25 nm.*

In Fig 2., the behavior of the output conductance in a device with a BOX thickness of 400 nm considering the and neglecting the SHE is shown. It is shown in Fig 2. that a device with a thicker BOX do not present the g_D transitions due to the substrate effect and in counterpart, the transition due to the SHE reaches high values, indicating that devices with a thicker BOX presents an intense SHE.

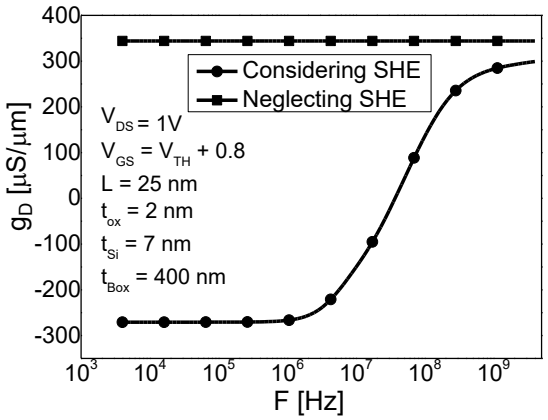

Fig.2. *Output Conductance at a function of the frequency for a UTB device with L = 25 nm.*

Fig 3. presents the g_D variation due to SHE for various BOX thickness and it shows that the effect varies nearly linearly with the BOX from 400 to 100 nm, from this point to the thinner ones, it presents an almost exponential behaviour in relation to the BOX thickness. Devices with thicker BOX present high thermal resistance [6] and, consequently, larger SHE, indicating the higher g_D variation due to the SHE. The penalty of a greater amplitude of g_D variation is to make the device more dependent on its operating frequency.

4. Conclusions

This work has evaluated the impact of the self-heating effect in the output conductance of UTB and UTBB SOI transistors. The overall analysis has been performed through AC simulations and it has been observed that devices with a thinner BOX present a g_D variation due to both substrate effects and SHE. The variation through SHE presents a nearly linear dependence on the buried oxide thickness, which seems to increase for devices with a thicker BOX. Finally, devices with a thicker BOX suffers from a more intense SHE and higher g_D variation.

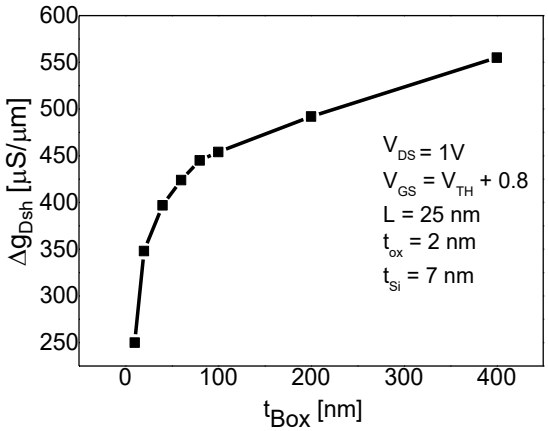

Fig.3. *Output Conductance variation due to SHE as a function of the BOX thickness for device with L = 25 nm.*

Acknowledgments

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Integrated Circuit Layout Using Educational Tools

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1. Abstract

Currently, it has been observed how the use of integrated circuits (IC) is important for technology development, they're present in practically all electronic devices used nowadays. The fact that allowed the development of integrated circuits was the domain of semiconductor materials, which led to the creation of the transistor, a key device for the integration of components into an IC. The electronics' industry focuses its efforts on always reducing the scale of the transistors to be integrated, this allows a greater amount of components to be inserted in the same IC. However, the difficulties of further scale reducing show that the efforts must be directed also to the layouts' development stage of these devices. Based on this scenario this paper aims to develop the layout of an IC CMOS, known as synchronous 4-bit counter using LASI (educational software), as a way to contribute to the dissemination of relevant knowledge to the IC design area. Farther, the simulations of the proposed circuits, performed through SPICE platform are also shown, ensuring the full functioning of the layout developed.

2. Introduction

Jointly with transistors, the Integrated Circuits are considered the most significant discover of the history in the electronic industry [1], because they have allowed the current growth and evolution of it. With the ICs production process evolution, the necessity to evolve the layout and design stages of these devices was arisen [2]. As the area of ICs design is a restrict area, with regard to educational issues due to high costs related to license acquisition of the robust commercial software, and the skilled labour is scarce (mainly in Brazil), there is a large requirement on training this manpower [3]. In order to approach this area to the university, so that rise the possibility of the graduation focused on ICs layout design, this paper aims the development of an useful CMOS (Complementary Metal Oxide Semiconductor) IC layout by using freeware educational tools. The software employed to make the layouts is called LASI (Layout System for Individuals), which is a program that requires of the user a good understanding of the employed technology and of the fabrication process, beyond that it also requires an understanding about the involved physics laws. LASI also have utilities that allows the error checking according to the rules imposed to each technology (DRC – Design Rules Checking) and the extraction of the circuit that can be simulated in SPICE (Simulation Program with Integrated Circuit Emphasis) based programs, which allows the simulation of the developed circuit in an integrated level. This paper also aims to demonstrate the needed stages to project an IC layout in order to ensure that it will be useful. However, it's important to highlight that the educational programs do not replace a commercial software, since educational programs cover the fundamental project requirements and demand that the students put efforts to understand the process and the variables involved in this (engendering knowledge), although do not provide the files and documentation required by the factory of integrated circuits (only commercial programs offer), but it includes all the simulations that promise circuit functionality.

3. Methodology

A. IC Design Flow

Aiming to facilitate and to disseminate easier and cheaper ways to learn and teach ICs design, as a way to bring it closer to the universities, a flowchart considering the main steps in the layout design of an IC was developed and is shown in Fig 1. These steps are meant to be used with the educational software LASI, so the designer student will be able to evolve well on the path of becoming a professional, considering that this sequence will demand the student to achieve the needed knowledge to understand the process of developing a functional IC.

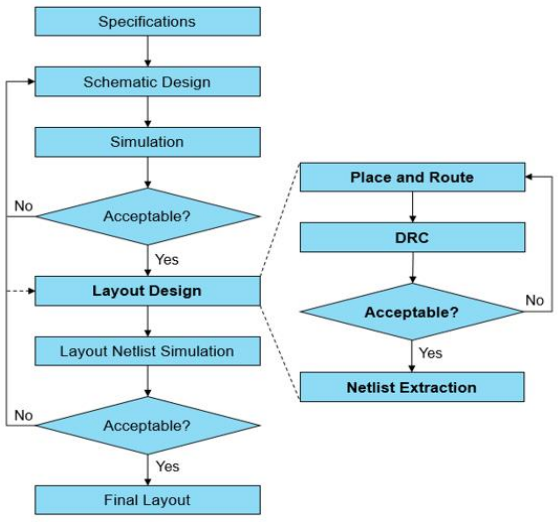

Fig.1. *Flowchart of designing sequence of steps.*

The first step is to check the specifications to define the technology, the transistors (sizes and threshold frequency) and the function of the IC.

The second step is the beginning of designing the schematic to verify if the circuit is going to accomplish its function and to find out which structures are going to be used on it. At this stage is necessary to run the simulation of what is being developed to see if it is acceptable or not. It is necessary to keep into this step until it gets acceptable (loop) so it is possible to jump to the next steps.

The third step is the actual layout's design and it consists in choosing the level of the layout (standard cell or full custom) and then in drawing the polygons to engender the transistors and the connections between the circuits. This stage is also a loop that the designer starts drawing the circuits, running from time to time the design rule check, to make sure there is no unacceptable construction on the layout, and then proceed to the netlist extraction.

The fourth step consists in evaluating the netlist in an external software (LTSPICE). Therefore, it is possible to know about micro and nano aspects that could affect the working of the circuit and about small level mistakes that could make it non-functional.

B. IC Development

Following the proposed sequence of steps a functional IC was developed. The structure chosen was the synchronous 4-bit counter. The Fig. 2 shows the first stage of this structure developed in LASI (the counter consists in four equal stages connected in cascade with logic gates dividing the frequency to the next stage). Each stage is designed with one flip-flop JK.

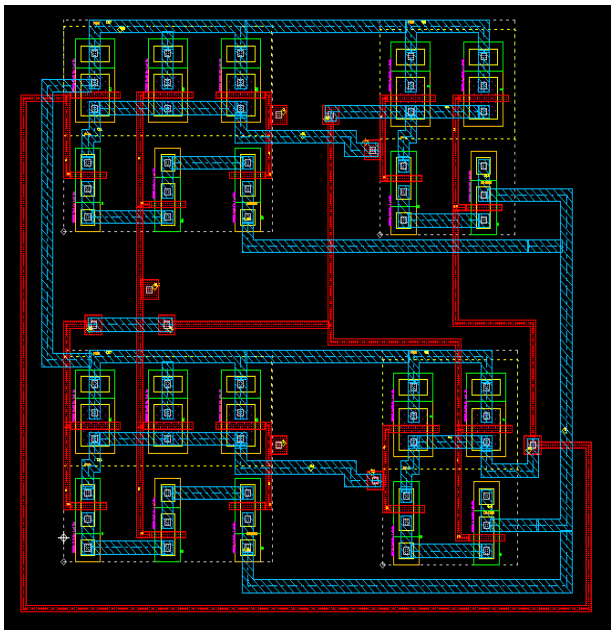

Fig.2. *Flip-flop JK (first stage of the counter).*

4. Results

After designing the counter, a set of simulations were carried out to make sure, it is a functional circuit. Using the LTSPICE it's possible to check if the circuit is functional. The Fig. 3 shows the behaviour of the circuit when a clock frequency is applied in the input where the first waveform is the applied clock and the next ones are the first and second stages of the counter.

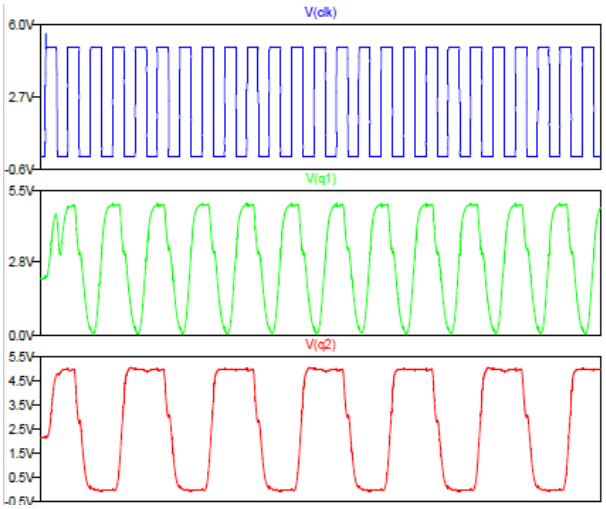

Fig.3. *Outputs of the counter with applied clock.*

5. Conclusions

The simulations show that the circuit developed works with good performance, considering the applied clock frequency.

The LASI software shows itself as an unexploited resource due to the lack of courseware material but at the same time as a powerful educational tool considering the amount of knowledge, it demands of the designer to engender a useful IC.

Using the sequence of steps proposed the feasibility of using LASI as a cheap first step in the learning process is increased.

Acknowledgements

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Improvement the harmonic distortion using the Diamond layout Style for MOSFET

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1. Abstract

The harmonic distortion is an important merit figure which is responsible for quantifying the how similar is an output electric signal of an amplifier, disregarding its voltage gain, in relation to the input signal applied, concerning the analog Complementary Metal-Oxide-Semiconductor (MOS) integrated circuits (ICs) applications. Hence, this paper aims to perform an experimental comparative study of the harmonic distortion between the Diamond MOS Field Effect Transistor (MOSFET) and Conventional one counterpart, regarding the same channel width, gate area and bias conditions. The devices were manufactured by using the 0.18μm Bulk Complementary MOS (CMOS) ICs from TSMC. The Integral Function Method was used to quantify the total harmonic distortion. The results show that the Diamond MOSFET with α angle equal to 135° can improve the harmonic distortion about 30% as compared to the one measured in the Conventional one counterpart.

2. Introduction

The non-standard layouts for MOSFETs is alternative way to improve the electrical performance of MOSFETs [1]. Besides, the layout strategy does not add any additional cost to the CMOS ICs manufacture process (low-cost solution) [1]. An example of this approach is the Diamond MOSFET (DM) that presents a hexagonal gate layout style [1].

The DM presents three different innovative effects, the Longitudinal Corner Effect (LCE) [1] that can boost its resultant longitudinal electric field (LEF) in relations to the conventional rectangular MOSFET (CRM) counterpart [with the same channel width (W) and gate area (A_G)]. The CRM present the same gate area than the DM its channel length L must be equal to (B+b)/2. Another effect is the Parallel connection of MOSFETs with Different channel Lengths Effect (PAMDLE), which is capable of reducing its effective channel length [L_{eff}=(B-b)/ln(B/b), where the B and b are its largest and smallest channel lengths] in relation to the CRM counterpart. Both effects (LCE and PAMDLE) can boost the DM drain current (I_{DS}) in relation to the CRM counterpart [1]. The other effect is the Drain Leakage Current (I_{LEAK}) Reduction effect (DLECRE), which is responsible for reducing its drain leakage current in relation to the CMR counterpart, due to the DM presents larger perimeters of the pn junctions between the drain and channel region than those found in the CRM counterpart, regarding the same W and A_G, and consequently the LEF lines in these junctions are reduced, although a larger perimeter of these junctions would tend to increase the I_{LEAK}. The result of these two effects happening simultaneously (reduction of the LEF lines and larger perimeter of the pn junctions between the drain and channel region) show that the effect of the reduction of the LEF lines is higher than the one due to the increase of the perimeter of the pn junctions between the drain and channel region.

Harmonic distortion is any deformation in the waveform of an output signal of an amplifier with respect to the input signal waveform applied, unless the voltage gain [2][3].

The Integral Function Method (IFM) is used to obtain the total harmonic distortion (THD) or linearity of an amplifier. This new technique does not need the obtaining of the frequency response of the amplifier, but only the characteristic curve of the output signal as a function of the input signal. In the case of an amplifier with only one MOSFET, it is necessary only the I_{DS} curve as a function of the gate voltage (V_{GS}) (DC electrical characteristics of MOSFET), in contrast of the Taylor and Fourier Methods [2]. Consequently, the IFM presents higher immunity to the noises of electrical measures of the devices than the method based on the Fourier series, and it presents a smaller error than that obtained regarding the calculation of the derivatives of the Taylor series [2].

Therefore, in this context, the motivation of this work, is to verify the total harmonic distortion (THD) behavior of DMs in relation to the CRM counterparts, focusing on analog CMOS ICs applications.

3. Experimental Results

The experimental measurements were performed at room temperature by using the Keithley 4200SCS device characterizer and Cascade Microprovider. The devices were manufactured by using commercial Bulk 0.18μm CMOS ICs technology from TSMC, via IMEC Free Mini@sic, Belgium. The dimensional parameters of the MOSFETs are presented in the Table 1.

Fig. 1 illustrates the log[I_{DS}/(W/L)] curves as a function of the overdrive gate voltage V_{GT} (=V_{GS}-V_{TH}) of the DMs and CRM (the reference).

Table 2 presents some electrical parameters (S: subthreshold slopes, I_{ON}: on-state drain current, I_{OFF}:

off-state drain current) and the digital figure of merit I_{ON}/I_{OFF} ratios of MOSFETs.

Table 1 - The MOSFETs dimensional characteristics (b=0.18µm).

MOSFETs	CM	DM (α=45º)	DM (α=90º)	DM (α=135º)
W [µm]	0.42	0.99	0.80	0.99
B [µm]	-	2.57	0.97	0.58
L [µm]	0.18	1.37	0.58	0.38
A_G [µm²]	0.08	1.36	0.46	0.38
W/L	2.33	1.18	2.49	4.29

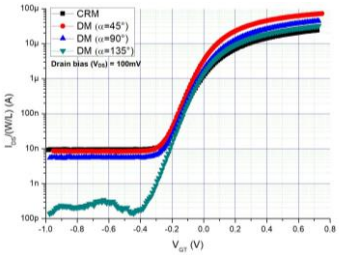


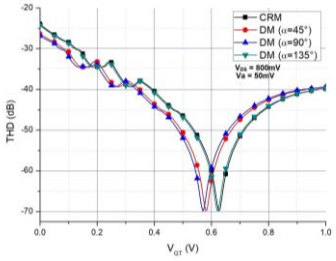
Fig. 1 – The Log(I_{DS}/(W/L) curves as a function of V_{GT}, regarding the drain bias (V_{DS}) of 100mV.

Table 2 – Some electrical parameters (S, I_{ON}, I_{OFF}, and V_{TH}) and the digital figure of merit I_{ON}/I_{OFF} ratios of MOSFETs.

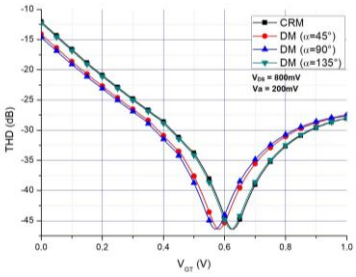
MOSFETs	CRM	DM (α=45º)	DM (α=90º)	DM (α=135º)
S [mV/dec]	120.0	99.7	96.0	90.0
I_{ON}/(W/L) [µA]	19.0	58.1	35.6	25.6
I_{OFF}/(W/L) [nA]	9.8	8.0	5.4	0.2
I_{ON}/I_{OFF}	1938.8	7262.5	6592.6	128000
V_{TH} [V]	0.476	0.440	0.471	0.473

Analyzing Table 2, we observe that the I_{ON} of the DM (α=45º) is highest value found between the other devices studied. This can be justified because the LCE and PAMDLE effects. Besides, the DM (α=135º) have presented the lowest I_{OFF} value of all devices considered in this study. This can be explained due to the DLECRE effect. Because of this fact, the I_{ON}/I_{OFF} ratio of if was 66 times smaller than the one measured in the CRM counterpart [3]. This study again reinforces that the LCE, PAMDLE and DLECRE effects in the DM structure can boost the electrical performance of the MOSFETs.

The THD of the MOSFETs were obtained considering two different of input signal amplitude (Va), i.e 50 mV [Fig. 2(a)] and 200 mV [Fig. 2(b)], regarding V_{DS} equal to 0.8V and varying its input DC level from the V_{TH} to V_{TH}+1V, and therefore the V_{GT} is between 0V and 1V.



(a)



(b)

Fig.2- The THD curves as a function of the V_{GT} of the DMs and CRMs, regarding Va=50mV (a) and Va=100mV (b)

Analyzing the Fig. 2, we observe that the THD of the different DMs are always better that the one found in the CRM counterpart. Besides, the THD of DM with α equal to 90º is 16 dB (about 30% regarding values of THD in dB) higher than the one measured in the CRM counterpart, regarding a V_{GT} of 0.58V and Va of 50 mV. Practically the same behavior was obtained regarding a Va of 200mV (14.9% for a V_{GT}=0.58V) This remarkable improvement in the total harmonic distortion can be justified by the LCE and PAMDLE effects [1].

4. Conclusions

This work performs an experimental comparative study of the harmonic distortion between the DM with different α angles and CRM counterpart, by using 180 nm Bulk CMOS ICs technology from the TSMC. Thanks to the LCE and PAMDLE effects, the THD of Diamond MOSFETs are always better than (for instance 30% concerning the DM with α angle equal to 90º) for the standard rectangular MOSFETs counterparts. Therefore, the hexagonal gate layout style for MOSFETs is an alternative device to be used in analog CMOS ICs applications.

Acknowledgments

We sincerely thank the IMEC for making the devices, CNPq, FAPESP and CAPES for their financial.

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Soliton Formation in Long Distance Optical Fiber Communication System

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1. Abstract

In this paper, we present the formation of Soliton in sigle-mode optical fiber (SMF), through simulation in Software OptiSytem 15.0 of the effects of SMF length as a function of Group Velocity Dispersion (GVD) and Self Phase modulation (SPM).

2. Introduction

The Soliton is an important application to optical communication systems, long-distance and that require wide bandwidth. This is a wave package that propagates without distortion over a long length of optical fiber [1], that is, keeps the same shape and width both in the time domain and the frequency domain, due to mutual compensation the non-linear effect of SPM and the linear effect of GVD respectively [2]. In long-distance fiber optic communication systems, losses are compensated by amplifiers, but the technological development of Sólitons systems is essential for the future of telecommunications [1]. In this sense we present here a soliton based optical communication system.

3. Materials, Methods and Theoretical Analysis

A. Simulation of Optical Soliton configuration

The block diagram of the optical communication system of 80 *Gb/s* for study of Soliton through the effect of SPM and GVD is shown in Fig. 1, where the Eq. (1) is solved numerically using the Split-Step Fourier Method (SSFM).

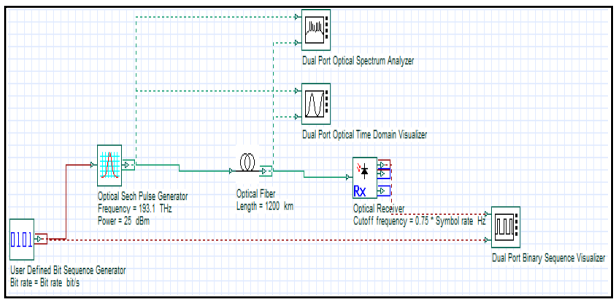

Fig.1. *Schematic for Soliton simulation.*

The transmitter consists of a Bit Sequence Generator with 8 bits (00001000) and an Optical Sech Pulse Generator at a frequency of 191.3 *THz* and input power P_{in} = 25 *mW*.

The SMF is configured for Polarization Mode Dispersion (PMD) with deterministic type birrefrigência, second order GVD β_2 = -20 *ps/km*, non-linear coefficient SPM $\gamma = 1.32\ w^{-1}km^{-1}$, core refractive index n_2 = 2.6e-20 m^2/W, effective modal area A_{eff} = 80 μm^2, wave-length λ = 1550 nm, attenuation α_0 = 0 *dB/km* and the length of SMF was arbitrarily varied for L_1 = 10 *km*, L_2 = 100 *km*, L_3 = 600 *km* and L_4 = 1200 *km* in the function Eq. (3).

The analysis of the results was done through the Dual Port Optical Time Domain Visualizer and Dual Port Optical Spectrum Analyzer in the time domain and the frequency respectively at the input and output of SMF.

B. Theoretical basis for simulations

Loss and scattering are factors that limit the pulse propagation in optical fibers. The SMF when subjected to a strong power in your electromagnetic field responds to non-linear way, so the SPM becomes more evident due to variations in refractive index. Already the GVD results from various modes of propagation and at different speeds, that cause Inter Symbol Interference (ISI) [1]. The Non-Linear Schrödinger Equation (NLSE) derived from the Maxwell's equations governs the pulse propagation in SMF [3, 4]:

$$\frac{\partial A(z,t)}{\partial z} + \frac{i\beta_2^2}{2}\frac{\partial^2 A(z,t)}{\partial t^2} = i\gamma\left|A(z,t)\right|^2 A(z,t) - \frac{\alpha A(z,t)}{2}, \quad (1)$$

were A is the amplitude of the wave, $\beta_2 = d^2\beta/d\omega^2$ determines the pulse dispersion in the quantum time. The coefficient of SPM $\gamma = 2\pi n_2/\lambda A_{eff}$. The attenuation [3]:

$$\alpha(db/km) = -\frac{10}{L}\log_{10}\left(\frac{P_{out}}{P_{in}}\right), \quad (2)$$

results of pulse propagation along the SMF and

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contribute to the reduction of output power [4]:

$$P_{out} = P_{in} e^{(-\alpha L)}. \quad (3)$$

Analytically, the soliton is a response by NLSE and is stable to disturbances of SPM and GVD.

4. Results and discussions

A. Effect of the Variation of the SMF Length without GVD and SPM Compensation

Fig. 2 shows the pulse at the at the SMF input in the time domain and the frequency. In this case I haven't suffered loss and scattering.

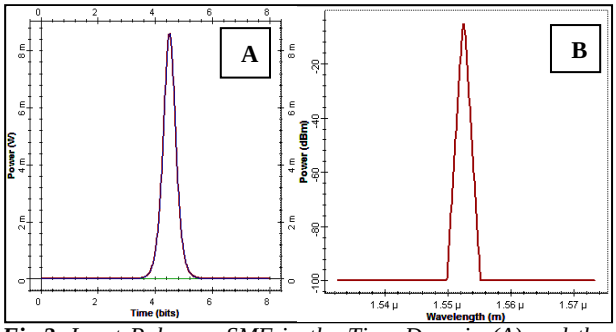

Fig.2. *Input Pulse on SMF in the Time Domain (A) and the Frequency Domain (B).*

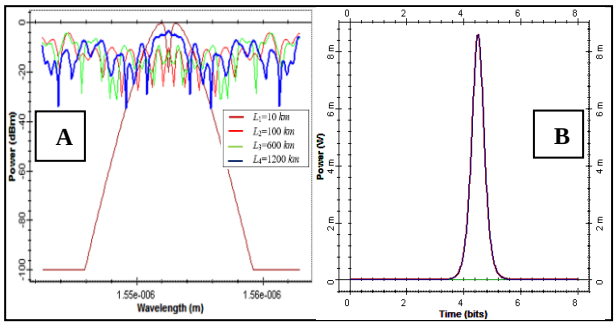

Fig.3. *Effect of the Variation of the Length of the SMF in the Frequency Domain (A) and Time Domain (B).*

Fig. 3 shows that with the increased length of SMF, modulations induced by SPM, which changed the shape of the initial pulse in frequency domain, but remained unchanged in the time domain.

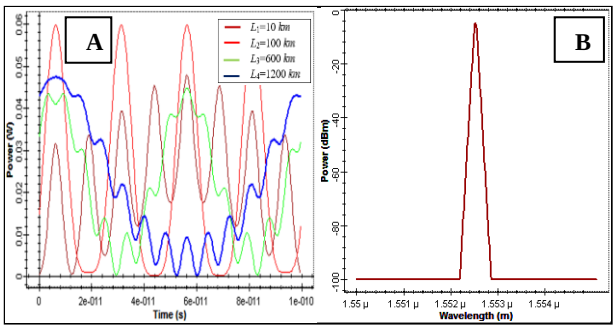

Fig.4. *Effect of the Variation of the Length of the SMF in the time Domain (A) and the Frequency Domain (B).*

Fig. 4 (a) shows that as the SMF length increases, the pulse is expanded by generating adjacent pulses in the time domain due to the increase in GVD, whereas fig. 4 (b) shows that in frequency domain the pulse shape remains the same.

B. Effect of the variation of the SMF length with GVD and SPM compensation

Fig. 5 shows that with compensation of GVD and SPM pulse kept your shape, width and breadth, when spread in the lengths L_1, L_2, L_3 and L_4 of SMF. In this second case occurred a mutual compensation of effects of GVD and SPM in both frequency domain and time domain respectively. In this second case occurred a mutual compensation of effects of GVD and SPM in both the frequency domain and the time domain respectively.

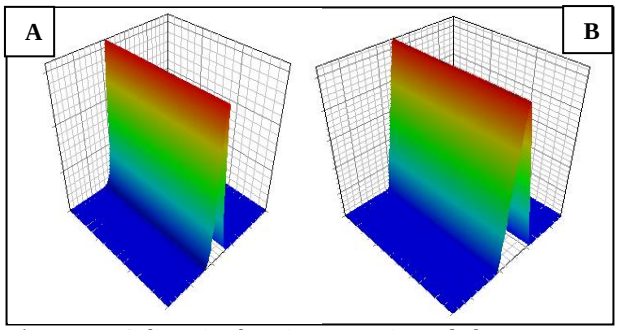

Fig.5. *3-D Soliton in the Time Domain and the Frequency Domain.*

That is, there was an overlap of signals for all the lengths of the SMF, resulting in a soliton.

5. Conclusions

In our communication scheme showed that the pulse can introduce distortions depending on the variation of the length of the SMF, but with mutual compensation of SPM and GVD got a soliton system both in the time domain and in the frequency domain. In future work we plan to analyze other parameter settings, such as attenuation and effective area.

Acknowledgments

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Degradation of the Output Characteristics of Junctionless Nanowire Transistors due to Negative Temperature Bias Instabilities

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1. Abstract

In the present work, we have analyzed the degradation by NBTI (Negative Bias Temperature Instability) in junctionless nanowire transistors (JNTs). The study was performed through 3D numerical simulations considering JNTs with different doping concentrations (N_D = $5x10^{18}$ cm^{-3} and $1x10^{19}$ cm^{-3}) as well as FinFETs whose results were considered as the reference. The analysis was done for transistors with different channel lengths between 20 nm and 100 nm biased at two different drain voltages. We obtained as a result the lower degradation by NBTI effect for JNTs device with higher doping concentration and higher drain voltage independently on the channel length.

Keywords- SOI, Junctionless, NBTI.

2. Introduction

The NBTI effect focuses on the reliability of the devices, especially for nanometric channel lengths [1]. This effect is associated with degradation of the gate dielectric of the devices along the time due to the presence of interface traps and is responsible for a degradation of the drain current (I_{DS}) and threshold voltage (V_{TH}) of the devices. Despite the NBTI degradation in MOS strucutres has been reported since the 60's, the importance of studies related to this effect has increased inversely proportional to the reduction of transistors channel lengths. In ultimate technological nodes, this effect has the potential to become a great reliability problem due to its deleterious effects. The degradation of NBTI, which is a problem inherent in P-type transistors, is one of the most significant problems of reliability and constant concern in CMOS technology for channel lengths below 130 nm [2]. Specifically, NBTI causes a systematic degradation in the electrical parameters of the transistor such as drain current, transconductance, threshold voltage and capacitance.

With the reduction in the size of the devices for extremely small nodes, the electrical characteristics of the devices are degraded by the so-called short-channel effects, since the control of part of the channel region charges starts to be done by the source and drain depletion regions. So that, several new technologies have been developed to reduce the short channel effects of the devices and to provide better electrical characteristics for extremely small technological nodes. One of these recent technologies consists of Junctionless Nanowire Transistors (JNTs) [3], which present several different aspects in relation to the conventional MOS, due to the absence of doping gradients between source and drain in relation to the channel. The JNTs work analogously to SOI accumulation mode devices. However, this is not properly an accumulation mode device [3], since the majority of the current flows through the body and not closer to the surface as in the SOI accumulation mode transistors. However, up to now, the effect of NBTI on such devices has not been deeply studied. Thus, this work aims to analyze the influence of NBTI on the electrical characteristics of junctionless transistors with different concentrations of dopants and channel lengths. The results have been compared to the ones shown by inversion mode FinFETs.

3. Devices Characteristics

The simulated structures present gate length (L) of 20, 25, 30, 50, 80 and 100 nm, silicon thickness of 10 nm and gate oxide thickness of 2 nm. The buried oxide thickness is 100, nm. JNTs present a constant doping concentration from source to drain, which has been varied from $5x10^{18}$ cm^{-3} up to $1x10^{19}$ cm^{-3}. In the case of FinFETs, the source and drain regions are doped with arsenic with a concentration of $5x10^{20}$ cm^{-3}, whereas the channel presents a boron doping concentration of $1x10^{15}$ cm^{-3}. All the simulations have been performed using Sentaurus TCAD [4] and models accounting for the carriers' generation and recombination, mobility dependence on vertical and longitudinal electric fields and bandgap narrowing have been considered. It is worth mentioning that the simulated I_{DS}-V_{GS} curves without considering the NBTI effect have been validated to the ones from [5].

3. NBTI Analysis

Among the various intrinsic wear mechanisms that contribute to the eventual failure or shorten the life of a metal-oxide-semiconductor (MOS) transistor, we have the Negative Bias Temperature Instability (NBTI). This is perhaps one of the effects that has the greatest potential to harm the development of new devices, since it demonstrates direct relation with the decrease of the channel length, causing the degradation of the threshold and current characteristics of a device due to the accumulation of positive charges at the channel / dielectric interface of the port and the generation of positively charged interface states. The above-mentioned mechanism is thermally activated and not linearly dependent on the electric field in the gate oxide [6].

In Figure 1, the I_{DS} x V_{GS} curves of a cascade of

junctionless transistors with variable L are presented. As a rule, the longer the channel length, the lower the current (in module) for the same V_{GS}, until the device cuts off. From the curves shown, it can be noted that the V_{TH} of the devices is reduced (in module) by reducing the channel length of the devices. This behavior is related to the increase in the influence of the short channel effects.

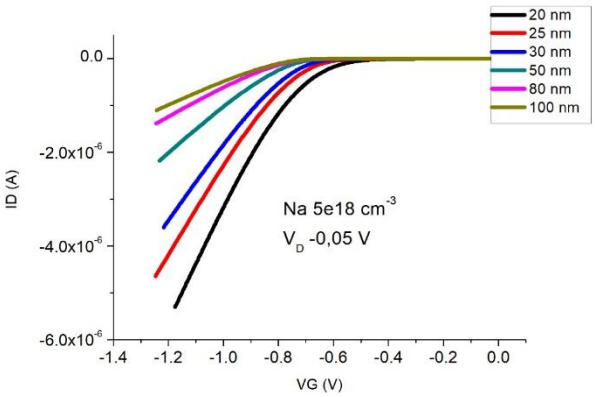

Fig.1. *Drain current as a function of the gate voltage for JNTs with doping concentration of 5 x 10^{18} cm^{-3} and drain voltage of -0.05 V.*

The on-state current of the devices has been extracted for a fixed $V_{GS} - V_{TH} = 1.0$ V neglecting the NBTI effect for all the devices as it can be seen in Figure 2. To extract the NBTI degradation in the I_{DS} also shown in the curves of Figure 2, the device has been biased at a fixed voltage overdrive for 10^3 s. As expected, when accounting for NBTI degradation, I_{DS} is always smaller (in modulus) than the currents not submitted and this effect. This phenomenon is associate to the increase (in modulus) of V_{TH} due to the presence of positive charges in the gate dielectric interface.

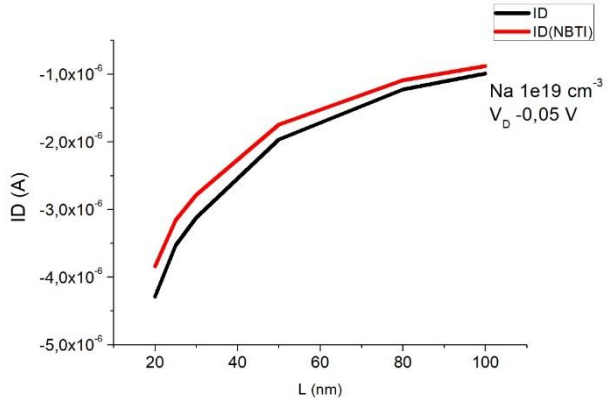

Fig.2. *Drain current as a function of the channel length for JNTs with doping concentration of 1 x 10^{19} cm^{-3} and drain voltage of -0.05 V.*

To analyze the NBTI influence, the threshold voltage variation (ΔV_{TH}) has been obtained as a function of L for the different devices as shown in Figure 3. When comparing the results of devices with L higher than 30 nm biased in the same V_{DS}, we can conclude that JNTs devices have a lower degradation by NBTI effect, in relation to the FinFET devices. This can be explained by the smaller electric field shown by junctionless transistors with respect to FinFETs of similar dimensions [7]. The same conclusion can be taken when comparing JNTs with different N_D as, when biased at same $V_{GS} - V_{TH}$ devices with higher N_D are farer from accumulation regime, resulting in lower electric field.

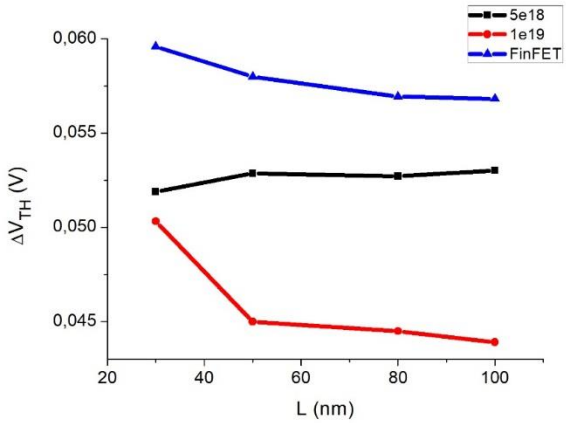

Fig.3. *Degradation of the threshold voltage versus the channel length for JNTs and FinFETs with drain voltage of -0.05 V.*

4. Conclusions

This work has shown, for the first time, the effect of the NBTI degradation on the drain current and threshold voltage variation of junctionless nanowire transistors with different doping concentrations. The results have been compared to the ones obtained for inversion mode FinFETs with similar dimensions at same bias. According to the results, JNTs presents lower NBTI degradation than FinFETs, which can be associated to the lower electric field. Additionally, the NBTI is lower for JNTs with larger doping concentration, since, for a fixed $V_{GS} - V_{TH}$, these devices are biased farer from accumulation regime and present lower electric field.

Acknowledgments

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Study of Biosensor Permittivity on a DG nTFET

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Abstract

In this paper, the study of permittivity on a double gate (DG) N-type tunneling field effect transistor (nTFET) for bio sensing purpose was done. The analysis was performed through two-dimensional numerical simulations. The sensing in the biosensor is due to a change in the ambipolar current of the transistor when biomolecules with different dielectric permittivity are immobilized in the bio element. The results show that the sensitivity of DG nTFET ambipolar current increase 3 order of magnitude when the permittivity of the bio element present on the drain underlap region increase from 1 to 20.

1. Introduction

The biosensor is a device that senses and transmits information from the biochemical domain into a chemical or physical output signal with a defined sensitivity [1], [2].

Biosensors devices are already present in personal healthcare, homecare, mobile diagnostics, environment monitoring. This devices attracts a great interest in recent years and a market of crescent investment for the future [3].

In this context, the fabrication of biosensors requires multidisciplinary research in chemistry, biology and engineering. Furthermore, for competitive and efficient biosensors, the devices requires low cost, fast response, simple operation, small size, low weight, high sensitivity and selectivity of the biomolecules targets.

In order to fulfill these requirements, various researcher groups studied biosensor based on field effect transistors (FETs) [4].

In this context, this work proposes the use of a double gate N-type tunneling field effect transistor (FET) for bio sensing purpose using the ambipolar current presented in these types of device [5], [6].

2. Device Characteristics

The biosensor have a fixed channel length (L_{SD} = L_G+L_U) of 50 nm, a gate length (L_G) of 35 nm, a drain underlap of length (L_U) 15 nm for better sensitivity in the ambipolar region [6], drain and source length of 100 nm each. The gate oxide thickness (t_{ox}) of 1 nm, a bio element thickness (t_{Bio}) of 10 nm, a silicon thickness (t_{Si}) of 10 nm and. The sensing of the biosensor device was performed varying the dielectric permittivity (K) in the bioregion in the range of K = 1, 4, 10 and 20. Fig.1 illustrate the simulated biosensor based on DG nTFET.

The drain and source are heavily doped with 10^{20} atom/cm^3 of arsenic and boron, respectively. The channel is lightly doped with 10^{15} atom/cm^{-3} of arsenic.

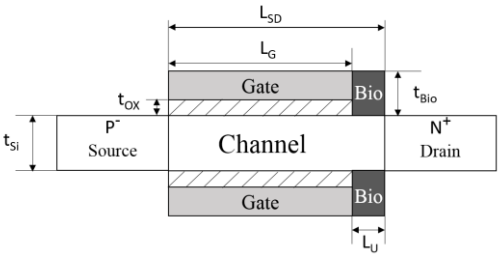

Fig.1. *Device structure of the biosensor based on DG nTFET.*

The device is simulated using the TCAD Sentaurus from Synopsys [7] with the dimensions previous mentioned. The parameters and polarizations used for the simulation were gate work function of 4.7 eV (i.e., Titanium Nitride), fixed drain voltage (V_{DS}) of 1V, a gate voltage (V_G) varying in the range of -3 to 3.

The models used in the 2D-numerical simulations are nonlocal band-to-band tunneling (BTBT), Shockley-Read-Hall (SRH) recombination and band-gap narrowing (BGN) model.

3. Analysis and Results

A. Effects of the permittivity

To study the DG nTFET working as an biosensor, the permittivity in the bio receptor need to change in order to simulate the binding of a target biomolecule, with a distinct dielectric permittivity, in the bio receptor. This change in the permittivity causes a perturbation in the behavior of the transfer curve of the device as shown in the Fig. 2.

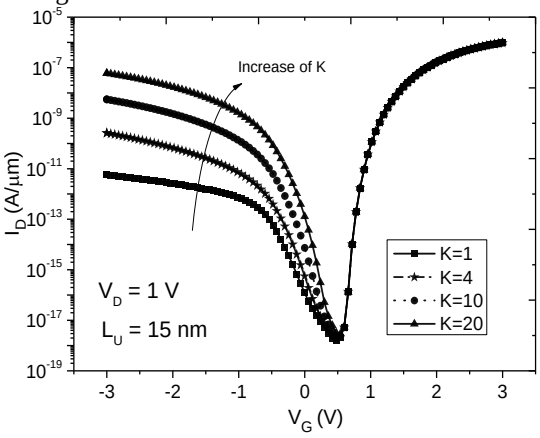

Fig. 2. *Drain current (I_{DS}) versus gate voltage transfer curve of DG nTFET for different values of K.*

Analyzing the ambipolar current of the nTFET, corresponding the current for a negative bias of V_G, is noticeable the increase of orders in magnitude of I_D from the lowest to the highest K. This increase is due the gate fringing field through the bio region that causes a larger bending of the bands closer to the interface channel-drain, increasing the ambipolar current [8].

Fig. 3 shows the bending of the bands closer to the interface channel-drain. Observing the bands limits, it is possible to notice the tunneling path decreasing as the values of K increase, implying in the rise in the tunneling current in the ambipolar region as observed in Fig. 2.

Moreover, analyzing the current for positive values of V_G (ON region of nTFET) the behavior of the current show no variation for the change in the bioregion permittivity. This implies that the biomolecule presence in the bioregion does not interfere in the ON region due the fact of it distance from the interface channel-source, the location of the local tunneling for positive gate bias [4].

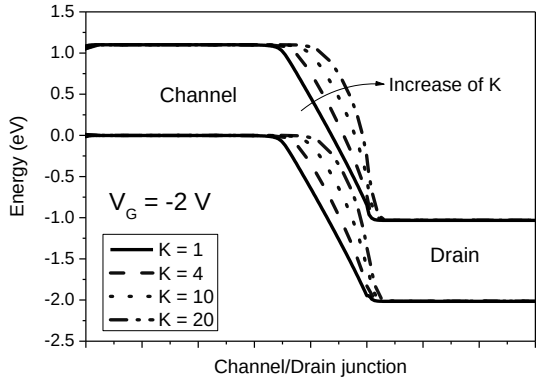

Fig. 3. *Energy band diagram for different values of K at 1nm above the interface channel-drain of DG nTFET.*

B. Sensitivity

The sensitivity parameter is defined as Sensitivity = $I_{D(K=n)}/I_{D(k=1)}$, where n is the value of the corresponding K. The sensitivity of biosensor is analyzed in the ambipolar region, where a higher variation with the permittivity was observe.

Fig. 4 illustrate the sensitivity in function of K, is possible to notice the increase of sensitivity of orders of magnitude between each values of K.

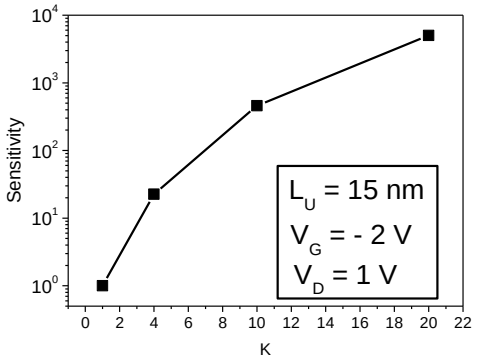

Fig. 4.*Sensitivity as a function of dielectric permittivity for biosensor biased at V_G = -2 V for DG nTFET.*

4. Conclusions

In this work, the study of biosensor permittivity on a DG nTFET was done in order to analyse the behaviour of the transfer curve of the device in a presence of a biomolecule with a distinct permittivity.

The biosensor studied with underlap of 15 nm presented high sensitivity for different values of K, and the best results were obtained for K = 20, making the DG nTFET device enable to bio sensing applications.

Acknowledgments

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Comparison between p-type and n-type silicon piezotransducers fabricated in CMOS technology

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***Abstract*—Two Eight terminals devices with exactly the same active area geometry, but designed in different layers with n-types and p-type silicon, were characterized in order to observe and compared the piezoresisitvity effect in different types of silicon. A controlled uni-axial stress between 5MPa and 70MPa was applied in both devices at the same time, the p-type piezotransducer shows a great sensitivity to the shear stress and a very small response to the other components of the stress, while the n-type silicon shows a sensitivity in all directions. The devices were monotonically integrated with the electric circuits to control the bias and sensing direction. The Piezotransducers were manufactured by CEITEC S.A. using a commercial CMOS process (XFAB 0.6µm) on a monocrystalline semiconductor wafer.**

1. Introduction

Monocrystalline silicon piezotransducer has a Gauge Factor up to two order of magnitude higher compared with similar strain gauges made of conductive metals foils. Also, silicon piezotranducers can be easily fabricated and integrated using the same semiconductor technology already developed for integrated circuits. Which allows several commercial successful applications as pressure sensor, accelerometers and force sensors to be developed [1, 2, 3].

Most of these devices are based on piezoresistivity effect, due to a simple integration with ICs and the linear response. The piezoresistivity effect is defined as change the resistivity due stress, it was first noticed in silicon by Smith[4] and modeled by Matsuda and Kanda[5, 6], those fundamental researches describe the silicon as an anisotropic material and the piezo-effect strongly dependent of the type of dopant in the semiconductor and doping concentration.

Sensitivity of the silicon piezotransducers is so strongly related to the orientation of the device and the dopant type, that those are the main design variables to be selected by sensors designers to application. For this work, we design and characterize two multi-terminal piezotransducers, with both p-type and n-type silicon active areas, using the available layers in the commercial XFAB 0.6µm CMOS technology, as shown in Fig.2. We compare the sensitivity for different uni-axial stress orientations and sensing directions.

2. The Piezoresistivity effect in multiterminal Silicon Piezotransducers

The piezoresistance is the change in resistivity due mechanical stress, and can be modeled by a set of empirical constants known as the First Order piezoresistive coefficients

Table I
First Order Piezoresistive Coefficients [$10^{-10}\mathsf{Pa}^{-1}$] .

FOPR [π_{ij}]	p-Type		n-Type	
	Smith	Matsuda	Smith	Matsuda
π_{11}	0.7	-0.6	-10.2	-7.7
π_{12}	-0.1	0.1	5.3	3.9
π_{44}	13,8	11,2	-1.4	-1.4

(FOPR): the longitudinal π_{11} , the transverse π_{12}, and the shear coefficient π_{44}. The values for the FOPR measured by Matsuda[6] and Smith[4] are presented in Table I.

A square four terminal device on a (100) silicon wafer is subjected to an uni-axial mechanical stress σ, as shown in Fig. 1. The crystal axis [100] is the reference direction, the device is orientated at angle φ and the stress is orientated at angle λ. An input Voltage V_{in} is applied on contacts 1 and 2 inducing a electric flux, an output voltage V_{out} is observed at perpendicular sensor-contacts 3 and 4. An analytic solution for stress sensible voltage output can be written as:

$$\frac{V_{out}}{V_{in}} \approx \frac{\sigma}{2}\left[\pi_{44}\sin 2\lambda\,\cos 2\varphi + (\pi_{11}-\pi_{12})\cos 2\lambda\,\sin 2\varphi\right]$$

Notice that the sensibility of devices aligned with the <100> crystallographic direction ($\varphi = 0\,, 90$) is related only to shear coefficient π_{44}, while the ones aligned with <110> ($\varphi = 45\,, 135$) is related to longitudinal π_{11} and traversal π_{12}. Then, two devices with different crystallographic orientation should be enough to determine the complete stress state at the surface. However, notice for p-type silicon, π_{11} and π_{12} are negligible compared with π_{44}[1, 4, 6], while FOPRs have an opposite behavior for n-type, therefor n-type devices have a increased sensibility if aligned with <100> direction while p-type devices are sensible if aligned to <110> direction.

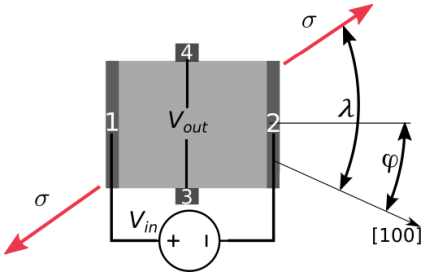

Fig. 1. Arbitrarily oriented silicon resistor

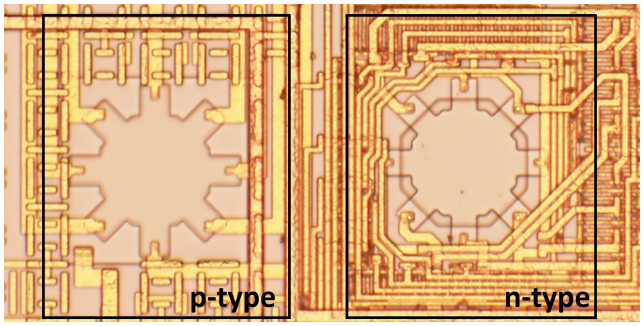

Fig. 2. Microphotography of integrated p-type and n-type Eight Terminal Silicon Piezotransducers (8TSP) and electronic circuit.

3. Design of the Piezotransducer Active Area

Instead of two four terminal devices with different orientations, a single 8 terminals device shown in Fig. 2 was designed and manufactured using a commercial technology, the XFAB 0.6um CMOS process. The n-type active area is n-well layer over the p-type substrate, while the p-type active area was designed using a diffusion layer with a p-type ion implantation over a n-well layer, therefor, n-type device has a lower doping concentration and a larger thickness compared with p-type device since n-well is deeper than the p-type implantation. Both devices have exactly the same geometry 8 point asterisk with a few modifications to avoid sharp angles and Design Rules problems. Some electronic circuitry to bias the devices, to control the bias/sensing direction and to filter the output signal were integrated in the same silicon die.

4. Experimental Characterization of the Device

Without external mechanical stress, the input Resistance in between opposite terminals is measured using the 4-point probes method: $R_{in}$of 2.96K$\Omega$was measured for n-type device while for the p-type device a R_{in} is 355Ω. Even is the n-well is deeper and the electron mobility is higher, the p-type device has a lower resistance since the doping concentration is much higher. Both devices are biased by a constant 5V supply voltage, however the p-type piezotransducer has a larger power consumption, since the input resistance is lower.

The devices were experimental characterized applying stress aligned with the main crystallographic (stress angle $\lambda = 0°$ for$\langle 100 \rangle$ direction and $\lambda = 45°$ for $\langle 110 \rangle$) using a four-point bending test. The output voltage were recorded for two different directions (φ of 0°, 45°), the results for other directions are not show since they are redundant. The measurements for the n-type device are shown in colored circles while for p-type are represented by colored triangles in the Fig.3. It is possible to identify a linear behavior in both the experimental measures. Notice for stress aligned with the $\langle 100 \rangle$ direction ($\lambda = 0°$), only the n-type device with the bias current orientated at angle φ 45° shows a significant change in the voltage output, while for stress at other direction direction ($\lambda = 45°$), both p-type and n-type with current at angle φ 0° shows a change at the output, and the p-type shows a greater sensitivity.

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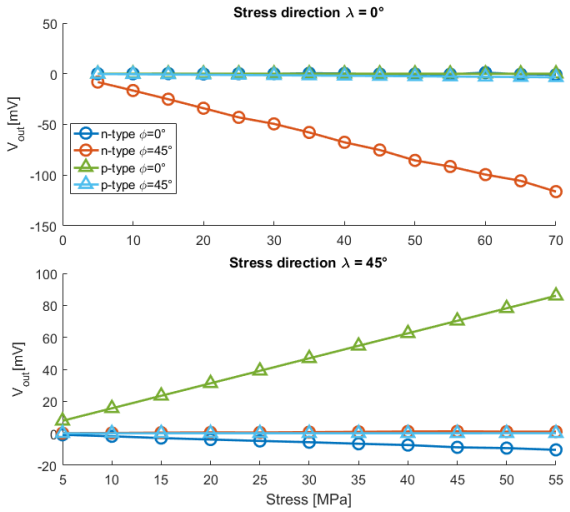

Fig. 3. Comparison between experimental measures for n-type and p-type Eight terminal piezotransducer

5. Conclusions

The p-type devices showed a great sensitivity to shear stress ($\lambda = 45°$) and very little variation when stress is aligned in longitudinal or transverse ($\lambda = 0°$), while n-type devices show variations in stress in all directions, being much more sensitive when stress is aligned with direction <100> ($\lambda = 0°$). The measurements are in accordance with the theoretical model and the values of the piezoresistivity coefficients.

Acknowledgment

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Prototypes of Microtransformers in MCM Technology

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1. Abstract

Several electronic devices such as implants and sensors network could benefit from compact transformers. Previous work demonstrated that transformers with very small dimensions can be constructed using MCM (Multi Chip Module) technology and ferrite cores. In this paper, the authors present new prototypes of microtransformers on a MCM platform developed at the Electronic Packaging Research Group at CTI. The goal of these prototypes is studying the effects of new winding configurations over key parameters of the transformers. The prototypes were characterized by means of coupling factor and inductance, showing good results.

2. Introduction

Following the scaling trend on electronics, there has been a great interest for PwrSiP (Power Supply in Package) and PwrSoC (Power Supply on Chip) devices. In the PwrSiP, the magnetic elements are packed together with the converter circuit, while in PwrSoC these elements are integrated to the circuit, leading to integrated bias sources [1]. However, building magnetic components directly onto/together with the integrated circuit demands complex and expensive deposition techniques that limit its commercial use [2]. Previous studies [1-4] make use of PCB's substrates. This limits the track to the submilimetric scale, i.e., 0.1 mm wide tracks can only be achieved in very calibrated fabrication process. Working on such critical condition compromises the reproducibility of the final devices.

MCM's (Multi Chip Modules) are electronic assemblies where several integrated circuits are mounted onto a substrate (usually alumina) to behave as a single circuit. The use of well known photolithographic technologies of the semiconductor industry leads to tracks that can scale down to micrometers.

The Electronic Packaging Research Group (NEE - Núcleo de Empacotamento Eletrônico) at CTI has the ability to fabricate MCM tracks down to 40 µm. This allows to a much greater scaling compared to PCB technology and, thus much smaller microtransformers.

Miniaturized magnetic circuits (i. e. microtransformers) using MCM-D (Multi Chip Modules – Deposition of thin films) fabrication technologies were already presented [5].

A prototype of an ultralow voltage oscillator for energy harvesting with a microtransformer using such technology was assembled and could work with only 30 mV [6].

This work presents new prototypes of microtransformers. The objective is analyzing the effects of new winding configurations and ferrite cores in the values of coupling factors, inductances and DC resistances.

The new prototypes are described on Section 3. Section 4 deals with the characterization technique of the prototypes and its results. Section 5 gives the conclusions.

3. Description of the New Prototypes

Two new prototypes were designed. The first one (project 2a) should receive a 14X9X5 N30 ferrite core from EPCOS with 14 mm external diameter thinned from its original height of 2.5 mm to 1.0 mm. The second one (project 2b) is intended to receive a 4.0X2.4X1.6 T38 ferrite core from EPCOS with 4 mm external diameter that had the height lowered from 1.6 mm to 0.5 mm. The height lowering of the ferrite cores enables to make more windings in the same core. The windings of both prototypes were made with aluminum wires of 31 µm diameter.

Project 2a has two windings groups. One of them enables the construction of spiral turns in groups of 10 turns in series up to 50 turns. The other group allows up to 40 turns in parallel. The prototype was assembled with 10 turns in series and 10 turns in parallel. Fig. 1 illustrates the final prototype.

Project 2b has the same configuration as 2a but the smaller diameter (4mm) leads to less turns around the core and more cores onto a single alumina substrate (Fig. 2). The prototype was assembled with 19 turns in series and 10 turns in parallel. The final 2b prototype is showed in detail in Fig. 3.

4. Electrical Characterization of the Prototypes

Prototypes were characterized regarding the inductance electrical parameters, ohmic resistance of the turns and coupling factor. This last one is the main figure of merit to be considered for microtransformer performance. Results are shown on Table I and II. Inductance and resistance were measured at 2 MHz, 1 V, while coupling factor was measured at 100 kHz, 1 MHz, and 10 MHz, 10 Vpp.

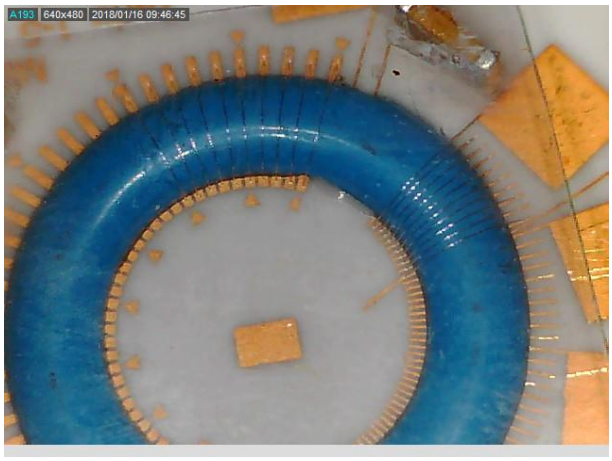

Fig.1. *MCM microtransformer project 2a with 10 turns in parallel (left) and 10 turns in series (right).*

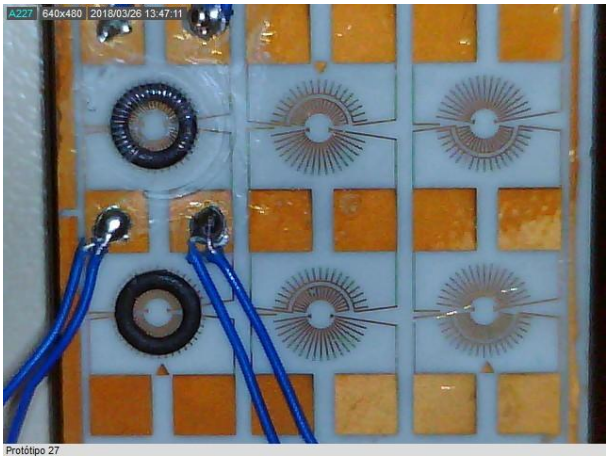

Fig.2. *MCM microtransformer project 2b.*

DC resistance and the inductance of the windings are defined mainly by the cross-section of the Au layer deposited onto the alumina substrate, i.e., layer thickness and track width. The performance of project 2b was also affected by the small thickness of the core.

Table I. *Electrical characterization results of the MCM microtransformer prototypes.*

Winding	Electrical parameter	Proj. 2a	Proj. 2b
Parallel windings	DC Resistance	1.12 Ω	1.43 Ω
	Inductance	61.8 nH	62.0 nH
Series windings	DC Resistance	5.08 Ω	5.71 Ω
	Inductance	6.37 µH	20.6 µH

Table II. *Coupling factors of the MCM microtransformer prototypes (in percentage).*

Project	Turns ratio	100 kHz	1 MHz	10 MHz
Proj. 2a	1:10	6.50	23.5	15.9
	10:1	73.8	84.7	97.3
Proj. 2b	1:19	4.70	22.3	15.1
	19:1	92.2	96.6	126

5. Conclusions

The fabrication of microtransformers using MCM technology was successful.

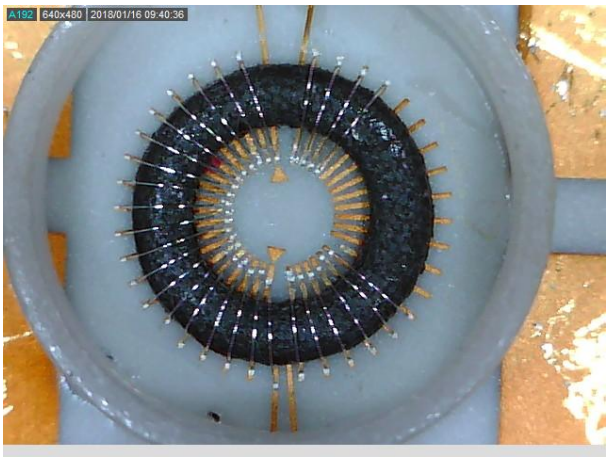

Fig.3. *Detail of MCM microtransformer project 2b with 10 turns in parallel (right) and 19 turns in series (left).*

Prototypes provided a coupling factor above 0.9 (90%), very close to the maximum found in literature for devices built on PCB and confirms previous results [5, 6]. It was noticed that putting turns in parallel brings no significant improvement on the inspected parameters.

As future improvement approaches it is expected that thicker Au layers for the MCM-D and wider tracks will reduce the ohmic resistance and provide a better coupling factor.

Acknowledgments

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Study of Process and Device Parameters for Improvement of Triple Gate Tunnel-FETs

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Abstract

This paper presents a study of process and device parameters for improvement of a triple gate pTFET. It is studied the influence of drain to gate underlap region, gate oxide thickness, carriers' lifetime and the use of Germanium source on device characteristics. The starting point was a real pTFET fabricated in imec/Belgium and the improvements were done by numerical TCAD simulation. The final results were a steeper subthreshold slope (SS), a lower leakage current (I_{OFF}) and a higher ON drain current (I_{ON}).

Keywords: TFET, FinFET, device optimization, simulation.

1. Introduction

As Moore's Law gets closer to its limits, new devices have been increasingly studied. Tunnel Field Effect Transistor (TFET) is one example of device that, despite of being structurally compatible with MOSFET fabrication, it works by a very different conduction principle: the quantum mechanical tunneling and, thus, provides the possibility of obtaining a SS smaller than 60mV/decade at room temperature, which is a physical limitation of MOSFETs [1]. However the silicon TFET presents low ON drain currents (I_{ON}) and degraded SS due to high Trap Assisted Tunneling (TAT) [1].

This work starts with the numerical simulation, using TCAD Sentaurus program, of an experimental triple gate Tunnel-pFET fabricated in imec/Belgium. The TFET is then improved and tested by simulation to estimate the gains in performance of them separately and combined together.

2. Device Characteristics and Simulation

The Tunnel-FET used in this work presents the following characteristics: the active region is made of Si and it has an effective channel length (Lch,eff), width (WFin) and height (HFin) of 150nm, 40nm and 65nm respectively. The buried oxide is silicon dioxide (SiO_2) and is 145nm thick, the gate oxide is composed of SiO_2 and HfSiON (high-k dielectric), with an EOT of 2nm, and the gate metal is made of TiN (workfunction of 4,68V).

The doping profile was always considered uniform. Source and drain regions were heavily do ped with a concentration of 10^{20} atoms/cm^3, with arsenic and boron respectively, and the channel was lightly doped with a concentration of 10^{15} atoms/cm^3 with boron as the tunneling effect requires junctions as abrupt as possible [1]. The resulting device is a PIN junction of a P-channel TFET.

The model of the geometry already with the numeric mesh in TCAD Sentaurus Device simulator can be seen on Fig. 1.

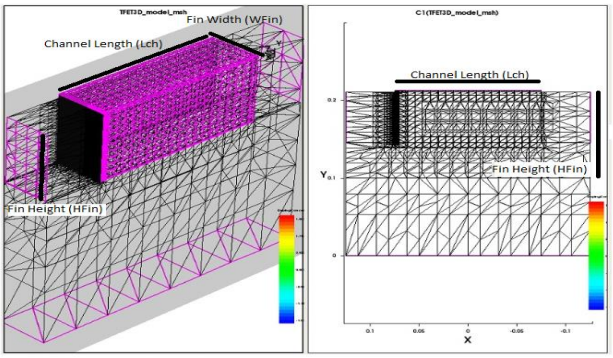

Fig.1. *Geometry and numeric mesh of the TFET device.*

The Band to Band model based on Kane's formula and WKB approximation with non-local path was activated to simulate the tunneling current. To simulate TAT and drift-difusion recombination currents that defines Ioff, it was used Schenk's model of carriers' lifetimes, using non-local path and a field enhancement factor to account for the TAT effect [2], in the device simulation program TCAD Sentaurus SDE.

3. Results, optimizations and discussion

A. Comparison with experimental results

The simulated results follow the same experimental behavior, except for the region between -1V and 0V of the experimental curve as the data in this region is not valid due to the limits of the measurement equipment (Fig. 2, where Ids is the drain current and Vgs is the gate voltage). The error between both curves is never above 1 order of magnitude, excluding the invalid region.

B. Reduced EOT and gate to drain overlap

Reducing EOT from 2nm to 1nm improves the gate to channel electrostatic control and makes the electric field stronger on the tunnel junction, raising I_{ON} current and improving SS (Fig. 2).

The presence of the underlapped region from gate to drain suppresses the ambipolar current, which also leads to a slightly better SS and I_{OFF}, as reported in [3] (Fig. 2).

C. Increasing carriers' lifetimes

A smaller concentration of defects and impurities that cause TAT can be simulated by increasing the carriers' lifetimes, which physically would correspond to a better fabrication process. Here, the lifetimes were increased in 5 times, leading to a steeper SS [2] (Fig. 3, where Ids is the drain current and Vgs is the gate voltage).

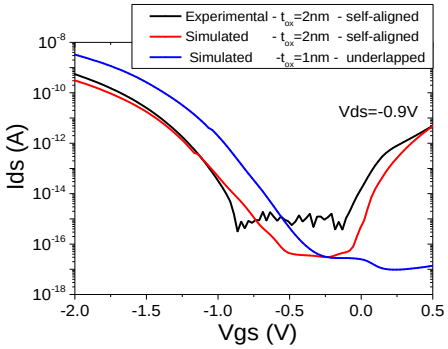

Fig.2. *Drain current (Ids) as a function of gate voltage (Vgs) of the experimental device and of the simulated devices: EOT=2nm and reduced EOT with underlap.*

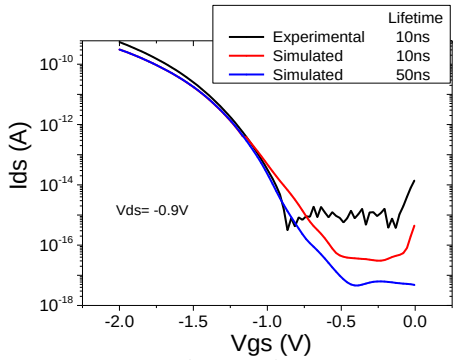

Fig.3. *Drain current (Ids) as a function of gate voltage (Vgs) of the experimental and of the simulated devices, with different lifetimes.*

D. Germanium source

By replacing silicon with germanium on the source, all parameters improve (Fig. 4) as this material has smaller effective carriers' mass and a smaller bandgap. Nevertheless, doing so should raise the concentration of defects near the junction, increasing TAT effect [4]. This effect on TAT was not taken into account on the simulations:

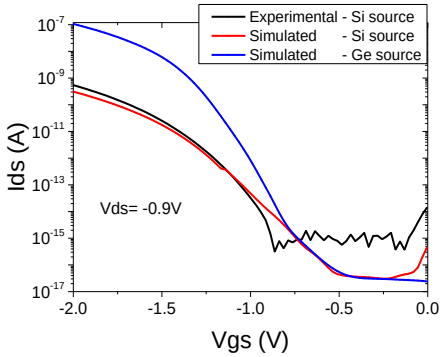

Fig.4. *Drain current (Ids) as a function of gate (Vgs) voltage of the experimental device, simulated ones with Si and Ge sources.*

E. All optimizations together

The drain current (Ids) as a function of gate voltage (Vgs) of the optimized device can be seen on Fig.5. WFin for the optimized device was reduced from 40nm to 20nm as this should improve the gate to channel electrostatic control, but simulations showed that this makes very little difference on the device's performance. Also, WFin must be at least 10nm because of SS degrading quantum mechanical effects [5].

Initially, the experimental device presented a minimum SS of 102mV/decade and none of the optimizations isolated could make it go below 60mV/decade. But with all of them combined together, SS reached its minimum value at 42mV/decade.

The I_{ON} current was about few nA at Vgs = -2V for the experimental device and reached about 1µA at the same bias condition for the optimized device.

The I_{OFF} current (measured at Vgs=0V) was about 1fA for the experimental device and reached 0.003fA with all the optimizations.

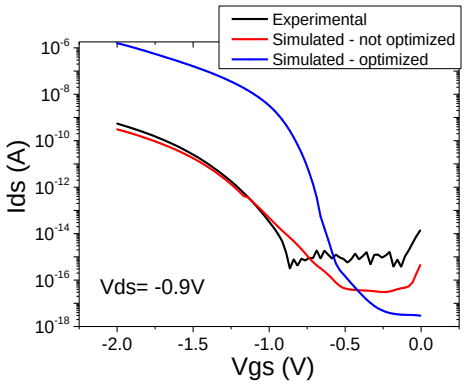

Fig.5. *Drain current (Ids) as a function of gate voltage (Vgs) of the experimental and of the simulated devices: with/without optimizations.*

4. Conclusion

The experimental silicon pTFET was improved using numerical simulation in this paper. The improvements that presented the most difference on I_{ON} current were reducing EOT and using Ge source, in such a way that I_{ON} was raised by 3 orders of magnitude. For I_{OFF}, the most important optimizations were the underlap between gate and drain and reducing the carriers' lifetimes (due to the reduction of defects concentration), reducing it in 3 orders of magnitude. SS improved from 102 mV/decade to 42 mV/decade with all the optimizations combined and the most important ones in doing so were using Ge on source and reducing the concentration of defects.

Acknowledgments

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The Role of the Intrinsic Length on the Operation of PIN Diodes Solar Cells on SOI Substrates

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Abstract— **This work demonstrates the use of PIN diodes fabricated in the substrate of SOI wafers, operating as solar cells in the conversion of solar energy into electricity. The research focuses on the relation between the device intrinsic length and what it provides in terms of efficiency and fill factor, fundamental parameters for the solar cell characterization. The studied cell has shown efficiency of about 7% to 8% and fill factor with average about 80%.**

Keywords– PIN Diodes; SOI Technology; Solar Cells.

1. INTRODUCTION

When PN diodes reversely biased are exposed to the sunlight, they can absorb and convert solar spectral power into carriers and current. Part of the energy of the incident photons is transferred to the carriers that form covalent bonds in the PN depletion layer, forming electron-hole pairs. These carriers are attracted to the P and N-type regions, depending on their charge and start to contribute to the reverse bias current. If the silicon layer thickness is thin, the PN diodes can be applied as light detectors of small wavelengths (usually blue and violet), whereas if the thickness is thick enough, they can be used as solar cells, to the conversion of sunlight into electricity [1,2].

When applied as solar cells, the diode depletion region becomes extremely important, since the carriers are generated in this region. Thus, it is possible to improve the performance of the PN diodes, by introducing a lightly doped region, so-called intrinsic region (with length Li) between P and N turning themselves into PIN Diodes [3]. These devices can enlarge the depletion region and work to obtain more current and more efficiency as it operates as a solar cell.

The PIN diodes can be fabricated in the conventional bulk silicon technology. However, when such devices are used to provide the energy of ultra-low-power (ULP) circuits, the integration between solar cells and circuits may be harmed, as ULP circuits fabricated in bulk silicon wafer can present many problems in order to keep the performance like parasitic capacitances and electric current leakage. So that, different technologies were developed, being one of the most promising, the SOI (Silicon-on-Insulator), which consists on applying a buried layer of silicon oxide between the active region of the silicon wafer and its substrate.

The mentioned technology ensures better electrical features for various devices due to the isolation provided, between substrate and active region, reducing current leakage and parasitic capacitances, at the same time, it allows higher density of integration. Therefore, one could use the SOI technology wafer, to produce PIN diodes on its substrate operating as solar cells to obtain electric power and send it to the upper layer to supply energy any other electronic devices as transistors, making it an autonomous system [4].

However, up to now, there are few works on available literature aiming the study of PIN diodes fabricated in the substrate of SOI wafers. Indeed, these devices should present Li large enough to provide energy to the circuits in the active region and small enough to occupy the minimum die area. Therefore, this work aims to determine how the intrinsic region length influences the PIN diodes performance acting as solar cells, establishing if there is on optimum intrinsic length to improve the device performance. The analysis has been performed through the evaluation of the efficiency and fill factor of the devices. The analysis has been based on numerical simulations obtained through Synopsys Sentaurus TCAD [5] simulations, validated from experimental results [6,7].

2. DEVICES CHARACTERISTICS

In order to evaluate the electric properties of PIN Diodes, 2D simulations were performed at Synopsys Sentaurus TCAD [5]. Models accounting for the mobility dependence on vertical and longitudinal electric fields, carrier's generation and recombination and bandgap narrowing have been considered in all the simulations. The simulations were validated to the experimental data from [7] and considered physical structures similar to the ones from experimental devices from [8], with the exception of the device width (W), which has been considered equal to 1 µm. The simulations were performed with ungated devices with Li varying from 1 up to 22 µm where the P and N regions present doping concentrations of 1 and $4x10^{20}$ cm^{-3}, respectively, and the intrinsic region presents P-type doping of $1x10^{15}$ cm^{-3}.

3. INTRINSIC LENGTH ANALYSIS

After validating the curves with the experimental data, we started with simulations with the device operating as solar cell. Fig. 1 shows the current as a

function of the cathode voltage (I_D-V_D) applied to the PIN diodes for different Li. Although the I_D-V_D of the devices have been obtained for a voltage range of -1 V to 1 V, the power only is positive for the voltage range between ~-0.1 V and 0.4V, indicating that out of this interval the diodes consumption is larger than energy generation.

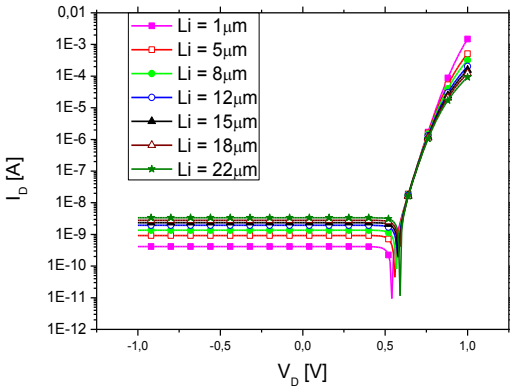

Fig.1. *IxV curve in logarithmic scale.*

From the I_D-V_D characteristics, it is possible to obtain the I-V pair, for which the maximum power (Pmax) is generated by the devices. The incident power and Pmax are presented as a function of Li in Fig. 2. To obtain the fill factor (FF), the maximum power supplied by an ideal device can be obtained by multiplying its open circuit voltage (Voc), obtained as V_D for $I_D = 0$, by the short current (Isc), which is the minimum I_D observed for negative V_D. The curves of Voc and Isc are also presented in Fig. 2 for the studied devices.

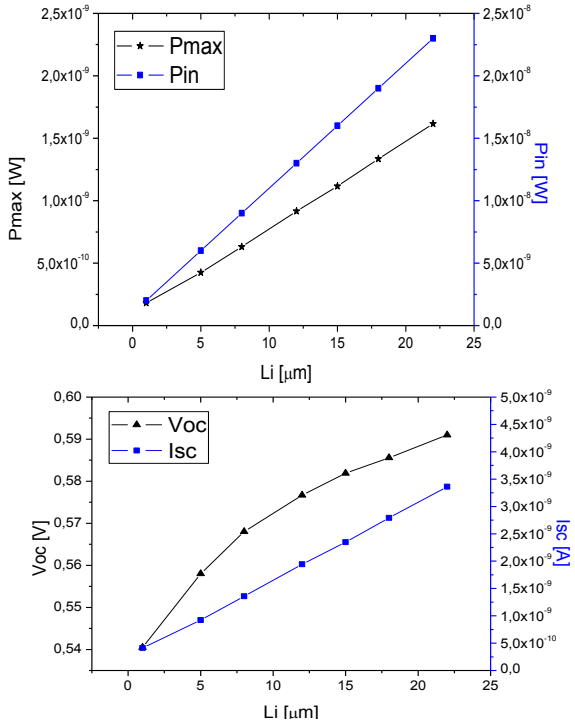

Fig.2. *Power curves, with maximum Power the device could obtain and the Pin (Incident Power), and the curves of Isc x Voc.*

The fill factor is given by ratio between the maximum power supplied by the devices by the maximum power of an ideal diode. Through the simulations performed it is possible to note that the intrinsic length has an important role in the characteristics of the devices. This parameter represents the efficiency in the conversion of the absorbed energy. The fill factor is presented as a function of Li in Fig. 3. As one can note, FF presents aa increase with Li up to Li = 7 µm and degrades for larger intrinsic lengths. This behavior is associated to the amount of carrier generated in the depletion layer and its efficiency in reaching the P and N junctions. For smaller Li, a lower amount of carriers is generated due to the smaller depletion depth, whereas for larger Li, a significant part of the generated carriers are recombined before reaching the P and N regions, diminishing the current and reducing FF. This phenomenon is associated to the carrier diffusion length, which is estimated to be in the order of 9 µm for the studied devices [8]. For that reason, it can be concluded that the optimum Li for the devices under analysis is close to 7 µm. The efficiency of the devices is also presented in Fig. 3 and slightly decreases from 9% down 7% when increasing Li from 1 to 22 µm.

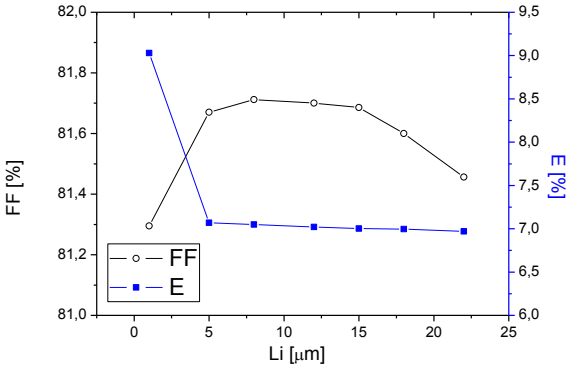

Fig.5. *The Efficiency and Fill Factor curves (ungated devices).*

4. CONCLUSIONS

The simulations of the PIN diodes operating as solar cells showed that the best operating relation of the devices was obtained for Li of 6 to 8 µm, where the best relation between efficiency and fill factor was obtained.

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Development of ADC ΣΔ in Conventional CMOS Technology Using Radiation Hardening Techniques

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1. Abstract

Based on research on the state-of-the-art ADCs ΣΔ (Analog to Digital Converter Sigma/Delta) over the past five years, it has been noted that ΔΣ modulators constructed with the RC continuous-time technique have increased. Especially in applications where less power consumption and higher conversion speed are required [3,7,9,10,12,14].

Also joining the state-of-the-art research on ionizing radiation tolerant ADCs, [19,20,21] the development of an ionizing radiation tolerant ADC was proposed for application in the area of space instrumentation.

The technical specifications of this ADC ΔΣ are: Second order modulator, single-bit, RC continuous time, 1kHz bandwidth and 16-bit resolution.

The techniques of radiation tolerance would be in a first step by design, at the layout level with the adoption of the ELT (Enclosed Layout Transistor) technique.
Numa segunda etapa a proteção será também por processo adotando-se a tecnologia SOI (Silicon On Insulator). In a second step the protection will also be by process adopting SOI (Silicon On Insulator) technology.

2. Introduction

The ADC ΣΔ is formed by two main blocks: (Figure 1) The ΣΔ modulator that receives the analog signal and converts it into a bit stream, and the digital filter, which converts the bit stream of the modulator into a "usable" digital number [1].

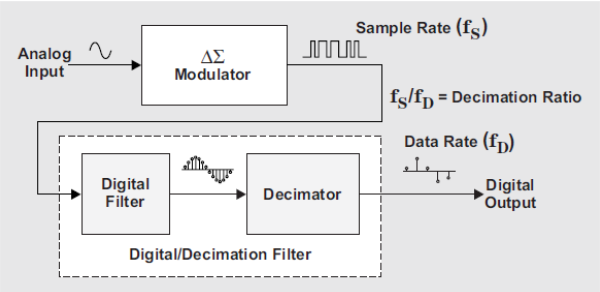

Figure 1 – A/D converter ΣΔ architecture [1].

The modulator ΣΔ (Figure 2) acquires many samples from the analog input to produce a bit stream. The Comparator (1-Bit ADC) works with clock (f_S), thus the quantization action produces a high sampling rate equal to the clock frequency f_S [1].

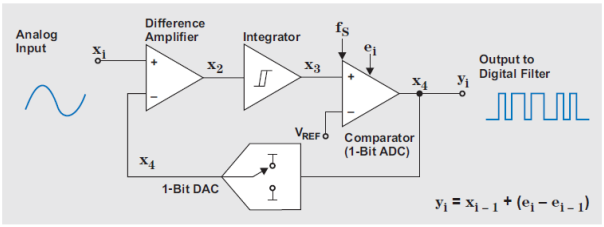

Figure 2 – Block diagram of a first order ΣΔ modulator, in the time domain [1].

The bit stream at the output of the modulator represents the analog input voltage. The ratio of the number of "1s" and "0s" represents the input analog voltage. In the time domain the output voltage of the 1-Bit DAC (Digital/Analog Converter) (X_4) is subtracted from the analog input voltage (X_i), providing an analog voltage X_2. This voltage is applied to the integrator, whose output progresses to the positive or negative direction. The slope and direction of the signal X_3 at the output of the integrator is dependent on the signal and magnitude of the voltage X_2. In turn, the voltage X_3 is compared to the zero volt reference voltage (V_{REF}), making the comparator output switch from negative to positive, or from positive to negative, depending on the comparison. The comparator output, voltage X_4, is applied to the 1-Bit DAC and the digital filter, signal y_i. When the comparator output switches from top to bottom or bottom to top, the 1-Bit DAC responds by changing the reference analog voltage applied to the subtractor. This creates a different voltage at X_2, causing the integrator to progress in the opposite direction. In the frequency domain (Figure 3) the ΣΔ modulator behaves as a high pass filter pushing the quantization noise to high frequencies [1].

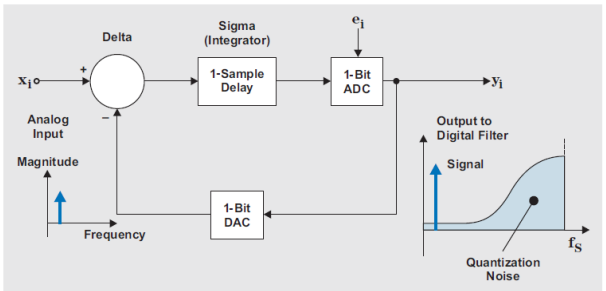

Figure 3 – Block diagram of a first order ΣΔ modulator, in the frequency domain [1].

The order of a modulator ΣΔ is determined by the number of subtractor (Δ) and integrator (Σ) blocks placed before the comparator (Figure 4) [1].

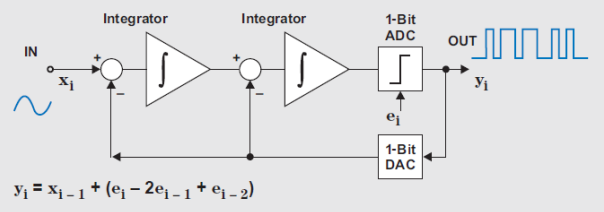

Figure 4 – Block diagram of a second order ΣΔ modulator [1].

How bigger the order of the modulator, for higher frequencies will be pushed the quantization noise, increasing the bandwidth of the input signal. The disadvantage is that the circuit becomes more unstable, making the design more complex [1].

The digital filter has four functions (Figure 5): 1) Averaging the "0s" and "1s" at the output of the modulator ΣΔ. 2) Filter the quantization noise by operating as a low pass filter. These two functions are done by the Sync3 Filter block. 3) Discard some of the many acquired samples (decimation). 4) Parallelize the bits forming a word usable by a processor. These two last functions are done by the Differentiator/Decimator blocks [2]. The Digital Filter of this work has 16 bits.

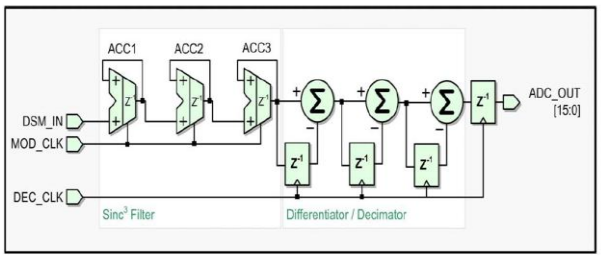

Figure 5 – Block Diagram of the Digital Filter [2].

3. Implementation

Figure 6 shows the complete layout of the ADC ΣΔ.

Figure 6 – Layout of the ADC ΣΔ.

In the lower left is the modulator ΣΔ. This was fully implemented with ELT transistors in the Xfab technology of 0.6 and of 5 Volts power supply. The digital filter is at the top. This was built with the library's digital cells and they are not ELT. A digital filter with digital cells with ELT layout is under development.

Every circuit has been developed and extensively simulated with the Cadence design tool.

4. Future Works

Construct the entire ELT layout of the ADC ΣΔ (digital filter and pads). Develop the same circuit in SOI technology. Fabricate both circuits and perform comparative testing for robustness to ionizing radiation.

Acknowledgments

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Analog Performance of the Asymmetric Self-Cascode Composed by FD SOI nMOSFETs with Different Channel Widths

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1. Abstract

This paper evaluates the analog performance of the Asymmetric Self-Cascode structure composed by Fully Depleted SOI nMOSFETs concerning to the influence of channel widths of the transistors near the source and drain, through three-dimensional numerical simulations.

2. Introduction

The Self-Cascode is a well-known configuration of improving the analog characteristics of MOSFETs, and is composed by two transistors in series with short-circuited gates, operating as a single device [1]. Commonly, both transistors present identical channel doping concentrations. Based on this structure, an alternative configuration has been proposed, named Asymmetric Self-Cascode (A-SC), shown in Fig. 1, where the transistor near the source (M_S) presents larger channel doping concentration, and hence higher threshold voltage (V_{TH}) in comparison with the transistor near the drain (M_D) [2]. In Fig. 1, W_S (L_S) and W_D (L_D) are the channel widths (lengths) of the transistors near the source and drain, respectively. The total channel length is given by $L_S + L_D$, however since the threshold voltage of M_D transistor is smaller than the M_S, the device close to the drain has its channel already inverted for V_{GS} close to V_{TH} of the A-SC structure, reducing the effective channel length to only L_S [2].

The analog analysis concerning to the influence of channel lengths of the M_S and M_D transistors has already been addressed in [3]. The objective of this paper is to assess the effects of different W_S and W_D, aiming to reach the largest intrinsic voltage gain.

3. Devices Characteristics

The measured transistor has been fabricated in a 2µm FD SOI technology from UCLouvain, Belgium [4].

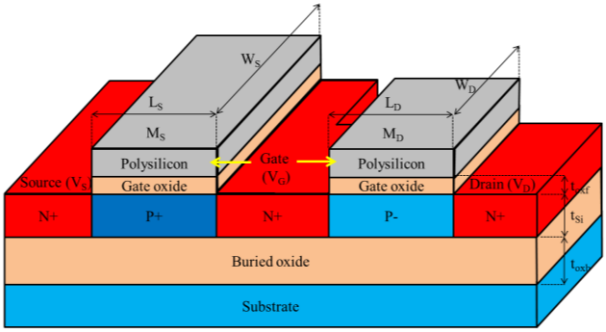

Fig.1. *Asymmetric Self-Cascode of FD SOI nMOSFETs.*

The single transistors present channel length of 2µm and channel width of 20µm. The gate oxide (t_{oxf}), silicon film (t_{Si}) and buried oxide (t_{oxb}) thicknesses are 31, 80 and 390nm, respectively. The M_S transistor features channel doping concentration of $6\times10^{16}cm^{-3}$, whereas the M_D transistor presents channel doping concentration of $1\times10^{15}cm^{-3}$ [4].

4. Results

Firstly, the parameters have been calibrated to fit the simulation results with the experimental measurements. Three-dimensional numerical simulations have been performed using Sentaurus Device software [5]. Fig. 2 presents the drain current (I_D) and the transconductance (g_m) as a function of V_{GS} for W_D=1µm varying W_S, extracted at V_{DS}=1.5V. The increment of W_S increases I_D and g_m in the whole V_{GS} range, since the M_S transistor is the dominant device in the A-SC structure. Fig. 3 evaluates the influence of W_D with W_S=1µm on the transfer characteristics. One can note at lower V_{GS}

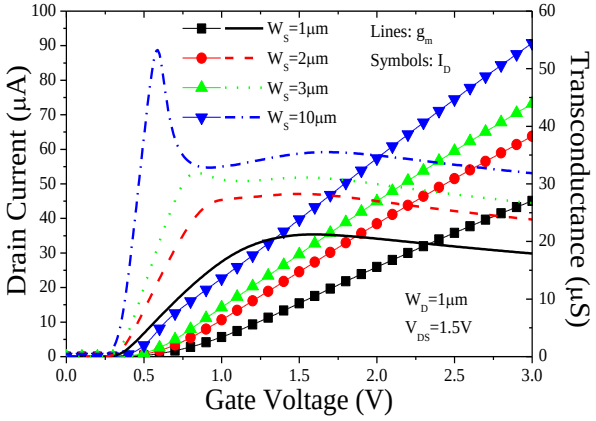

Fig.2. *I_D and g_m vs. V_{GS} at V_{DS}=1.5V for different W_S.*

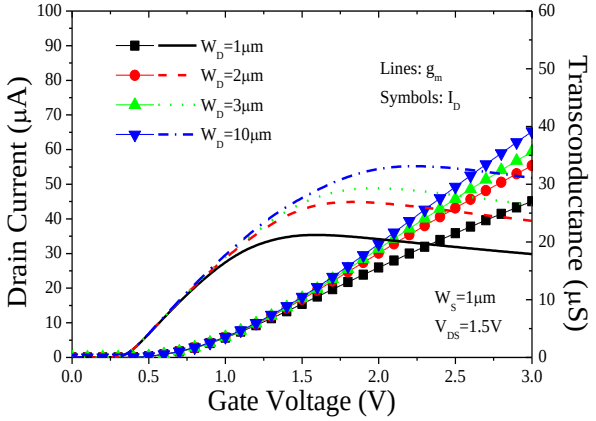

Fig.3. *I_D and g_m vs. V_{GS} at V_{DS}=1.5V for different W_D.*

that the increase of W_D does not affect I_D and g_m due to the larger electron concentration in the M_D, linked to its lower V_{TH}. As mentioned before, the M_S dominates at low V_{GS}. When V_{GS} increases, the M_D influences I_D and g_m, due to the similar electron concentrations in both transistors. The wider M_D, the larger I_D and g_m, since its resistance is reduced. In order to understand the two g_m peaks for the A-SC W_S=10µm; W_D=1µm in Fig. 2, the intermediate potential between M_S and M_D transistors (V_X) is presented as a function of V_{GS} in Fig 4 for W_D=1µm varying W_S. It is possible to observe a high V_X for V_{GS} close to V_{TH}, which implies in larger I_D and g_m. When V_{GS} increases, V_X considerably reduces, decrementing g_m. When V_X is stabilized, one can notice an increase of g_m due to the increment of V_{GS} until the moment where the mobility degradation and the similar electron concentrations in both M_S and M_D occur, reducing g_m. Also, the increase of W_S reduces V_X due to the lower M_S resistance. Fig. 5 exhibits I_D and the output conductance (g_D) as a function of V_{DS} for W_D=1µm varying W_S, extracted at gate voltage overdrive ($V_{GT}=V_{GS}-V_{TH}$) of 200mV. Since V_{GT} is reduced, the M_S controls the A-SC structure. This way, the increase of W_S increments both I_D and g_D. Based on Fig. 6, where I_D and g_D are plotted as a function of V_{DS} at V_{GT}=200mV for W_S=1µm and different W_D, one can observe that the increase of W_D slightly increments I_D, but reduces g_D. Fig. 7 presents g_m (A), g_D (B) and the intrinsic voltage gain ($A_V=g_m/g_D$) (C) as a function of W_D, extracted at V_{DS}=1.5V and V_{GT}=200mV.

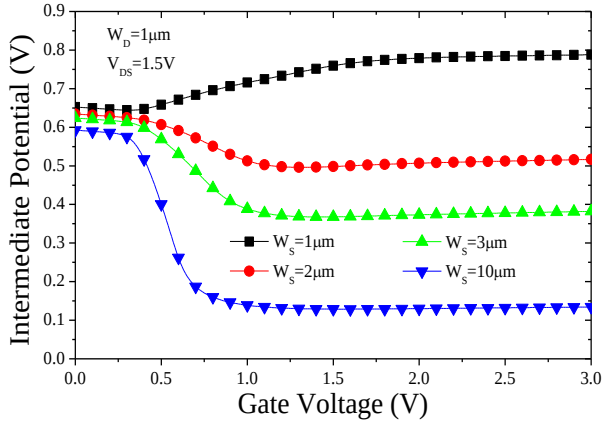

Fig.4. *V_X vs. V_{GS} at V_{DS}=1.5V for different W_S.*

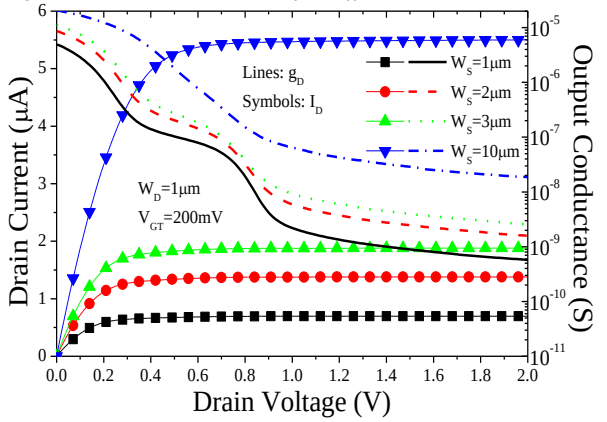

Fig.5. *I_D and g_D vs. V_{DS} at V_{GT}=200mV for different W_S.*

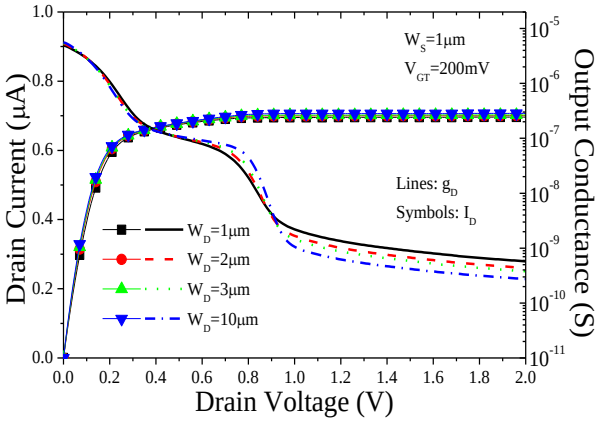

Fig.6. *I_D and g_D vs. V_{DS} at V_{GT}=200mV for different W_D.*

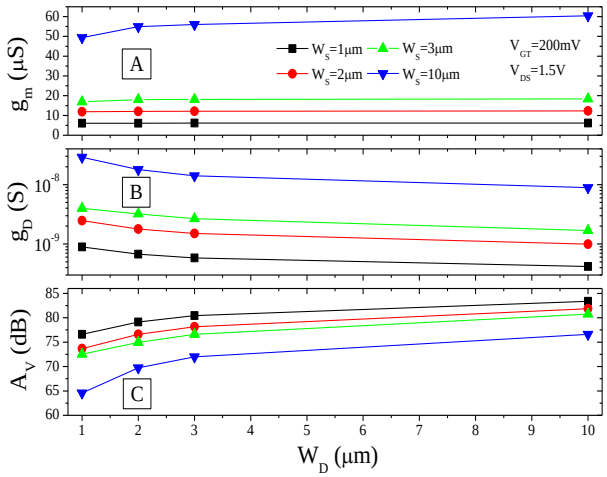

Fig.7. *g_m (A), g_D (B) and A_V (C) vs. W_D at V_{DS}=1.5V and V_{GT}=200mV for different W_S.*

One can note that the rise of W_D increments g_m, but reduces g_D, increasing A_V. When W_S is incremented, the increase of g_D is larger than the rise of g_m, reducing A_V. This way, the maximum A_V has been verified for the widest M_D transistor and narrowest M_S transistor.

5. Conclusions

This work has endorsed that the M_S dominates the A-SC conduction for all V_{GS}. However, at high V_{GS}, the M_D also impacts on the drain current flow. The increase of W_S has incremented g_m and g_D, reducing A_V, whereas the increase of W_D has slightly increased g_m, but reduced g_D, incrementing A_V. Summing up, the largest A_V has been obtained for the A-SC structure composed by the narrowest M_S and the widest M_D.

Acknowledgments

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Ground Plane Influence on Ge pFinFET Subthreshold Swing

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1. Abstract

This paper studies the ground plane (GP) influence on germanium channel pFinFET devices for different channel width. The results are based on the analysis of subthreshold swing for different GP doping concentrations and its position below the effective fin.

2. Introduction

It is well known that FinFET structure presents better electrostatic coupling between gate and channel which results in a better short channel effects [1]-[2]. The germanium (Ge) pFinFET presents the highest hole mobility compared to other materials [3].

This study proposes the analysis of the Ge pFinFET focusing on subthreshold swing (SS) performance. In addition, the GP doping concentration and its position below the effective fin are taken into consideration using TCAD simulation.

3. Devices Characteristics

Table I contains the parameters used on the Sentaurus TCAD simulations of Synopsys [4], considering the main dimensions and characteristics of simulated Ge pFinFET devices. The simulations were based on devices as in [5].

Fig 1. presents a p-type channel of FinFET structure and its main regions. The gate voltage (V_{GS}) was swept from accumulation to inversion regime (1 V to -0.5 V), stepped by 10 mV in linear region, i.e., drain voltage (V_{DS}) of -50 mV.

Table I – Main simulated devices characteristics

Parameter	value
fin width (nm)	20; 50 and 100
length channel (μm)	1
fin height (nm)	30
substrate doping concentration (cm^{-3})	$1x10^{15}$ (Phosphorus)
channel doping concentration (cm^{-3})	$1x10^{15}$ (Phosphorus)
ground plane peak doping concentration – Gaussian profile (cm^{-3})	$1x10^{17}$ to $1x10^{19}$ (Phosphorus)
drain and source doping concentration (cm^{-3})	$1x10^{20}$ (Boron)
gate oxide (nm)	1.5 (SiO_2)
metal work function (eV)	4.5 (TiN)

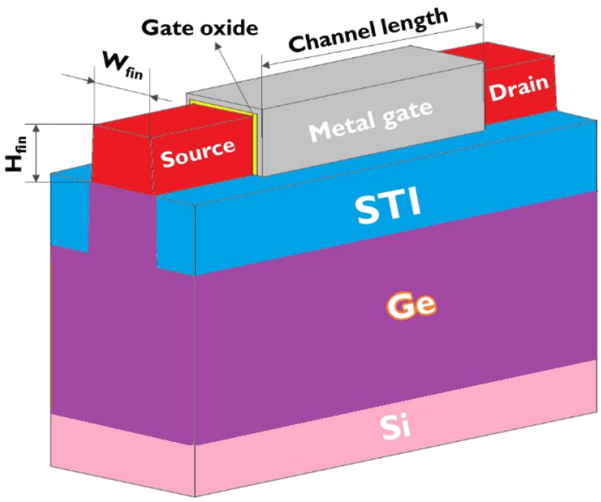

Fig. 1. Germanium FinFET structure.

There are two different viewpoints of the ground plane under investigation, as presented in Fig 2 and Fig 3, GP peak concentration and depth, respectively.

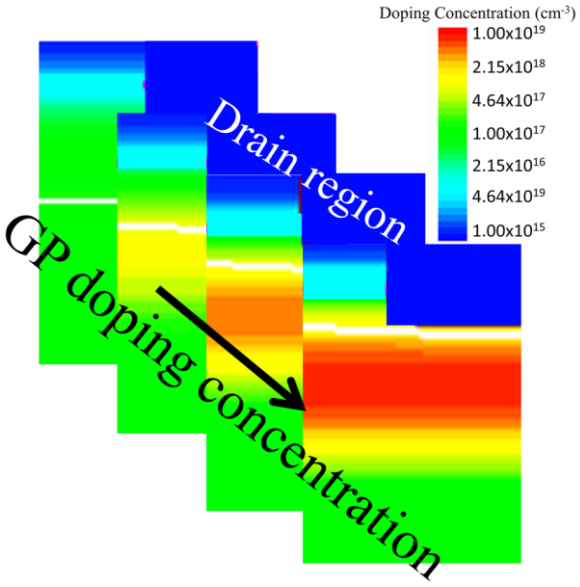

Fig. 2. Zoom out of longitudinal view from Ge pFinFET structure for different doping concentration values.

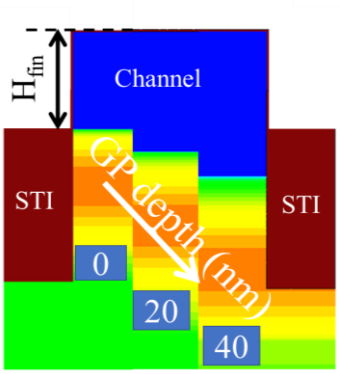

Fig. 3. Cross-section view from Ge pFinFET structure for different ground plane depth.

4. Results and Analysis

Fig. 4 shows the subthreshold swing as a function of fin width for Ge FinFET devices with different ground plane doping concentrations. It is possible to see that there is no significant impact of the GP doping concentration on the SS values. On the other hand, the subthreshold swing is clearly W_{fin}-dependent, revealing that the electrostatic coupling is more dominant, in other words, the narrowest device has better SS values compared to higher W_{fin}.

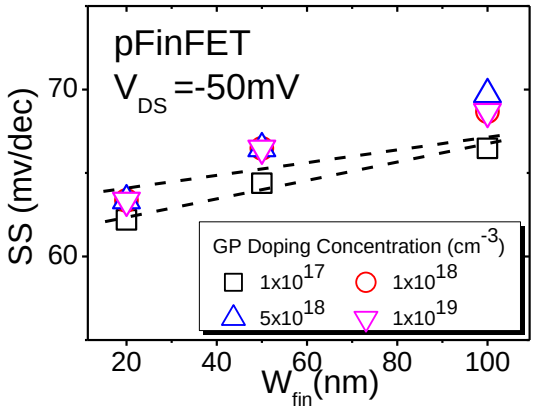

Fig. 4. Subthreshold swing as a function of fin width for different ground plane doping concentrations.

Fig. 5 presents subthreshold swing as a function of fin width for different ground plane (GP) depths. It is noticeable that there is a relevant influence of the depth in the subthreshold swing value. As the GP depth increases, the SS value for narrow fin is degraded and presents less dependence of the fin width. For larger GP depth there is a leakage current under the channel region that flows from the source to the drain, since the GP is placed away from the bottom of the fin, reducing its barrier isolation for drain and source regions [6]. In contrast, better electrical coupling can still be found for no ground plane displacement, i.e., GP depth of zero nm, whereby the SS value is lower for W_{fin} = 20nm.

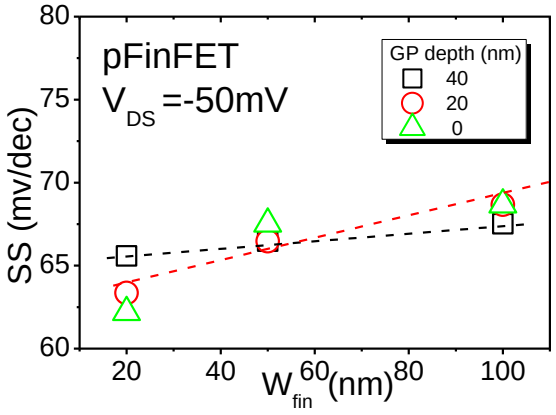

Fig. 5. Subthreshold swing as function of fin width for different ground plane depths.

5. Conclusions

This paper studies the ground plane (GP) influence on Ge pFinFET analyzing the GP doping concentrations and its position below the effective fin. As a result of this work, the relationship between subthreshold swing (SS) and width variation is presented in both cases, due to the electrostatic coupling domination. It was also observed that both GP doping concentration and GP depth variation affects the SS, but only the second one influences into the parameter degradation.

Acknowledgments

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Analysis of Illuminated PIN Photodiodes under Mechanical Stress

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1. Abstract

PIN photodiodes have presented many applications in the most diverse areas, from medical-laboratory studies to spatial observations. This study aims to evaluate the influence of mechanical strain on photosensors when illuminated by different wavelengths through the analysis of numerical simulations.

2. Introduction

The PIN photodiodes are fabricated in a silicon wafer and are composed by three regions, the "P+" and "N+" regions and between them an intrinsic "I" region that can be "P-" or "N- " type, with low concentration of impurities. When reversely polarized, the diode can detect incidence of light by an increase in its reverse electrical current. It occurs as the photons break the covalent bonds generating electron-hole pairs in the depletion layer [1]. In a PIN photodiode, its light-sensitive depletion area is expanded through the intrinsic region and becomes more sensitive to light.

3. The Mechanical Stress

The mechanical stress in semiconductor materials is generated through mechanical deformations and can be defined by the relative displacement in the crystalline lattice [2]. The mechanical stress is a straight forward tool that enables the improvement of performance on devices by increasing the mobility of carriers without interfering the dimensions of the device, leading to the increase of the electric current [3] and altering other parameters, such as the bandgap that is directly related to the photocurrent generation [4]. The mechanical stress changes the energy levels of the semiconductor, as seen in fig. 1, shifting the valley to lower energy levels (Δ_2) and it tends to be more occupied by electrons.

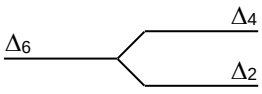

Fig. 1. *Silicon energy bands before and after stress.*

The lowering in the levels reduces the effective longitudinal (m_l) and transversal (m_t) masses of electrons in the plane, increasing its mobility as seen by eq. (1).

$$m^* = \left[\frac{1}{6}\left(\frac{2}{m_l}\right) + \left(\frac{4}{m_t}\right)\right]^{-1} \quad (1)$$

The division of the conduction band in the Δ_2 and Δ_4 valleys also causes the reduction in the rate of scattering electrons in the network. If the division between the Δ_2 and Δ_4 valleys is greater than the energy of the phonons, the chance of scattering is reduced significantly in addition to the increase in mobility of the electrons [5].

In unstrained silicon, the maximum valence band for holes is more complex. At room temperature, the holes occupy the upper two bands. A key point to achieve a high mobility of holes in the plan is to reduce the effective mass of the upper band, raising it and distancing it from the lower band [2].

4. Methodology

Through the numerical simulator Sentaurus Device from Synopsys [6], the PIN photodiode structure is analysed using two-dimensional numerical simulations, varying the dimensions of the device, the wavelength of the incident light and the applied mechanical stress.

For recombination, we used the models Shockley-Read-Hall (dependent on dopant concentration) and Auger with electron-hole generation. For mobility, the models Masetti (dopant concentration dependent), Lombardi, Philips unified mobility model, Caughey-Tomas for high saturation electric field and Conwell-Weisskopf for carrier-carrier scattering were considered.

5. Simulation Results and Discussion

The longer the wavelength, deeper the incident light penetrates the device and generates electron pairs [7]. Ideally the total quantum efficiency would be 100% if each incident photon generated an electron-gap pair, but the actual efficiency is limited by the photosensitive area, the reflections and recombination process [8]. The fig. 2 illustrates the influence of wavelength on quantum efficiency for silicon, from [4].

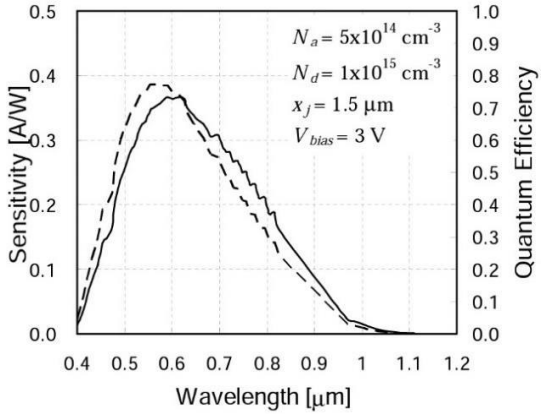

Fig. 2. *Sensitivity and quantum efficiency as a function of wavelength for silicon, from* [4].

The fig. 3 was obtained from a set of numerical simulations where the parameters previously mentioned are observed. We can verify that the wavelength influence in the electric current follows the same tendency of the quantum efficiency in fig. 2.

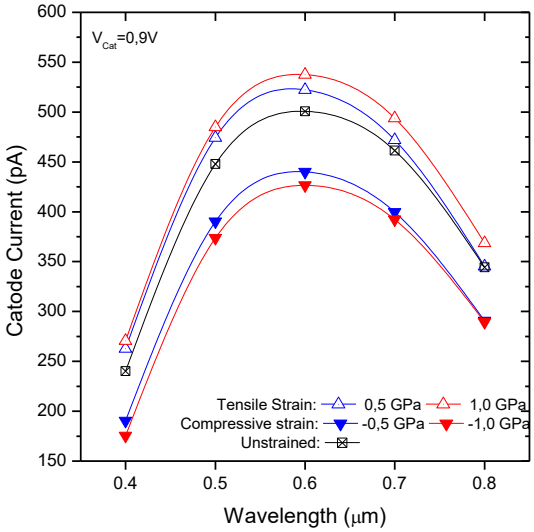

Fig. 3*. Cathode current as a function of the wavelength for tensile and compressive strains applied.*

The device used has an intrinsic P- type region. For this, the tensile mechanical strain produces an increase in electric current. The compressive mechanical strain produces a decrease in the electric current.

6. Mechanical Bending Setup Proposal

Experimental measurements with multiple mechanical stresses applied to the sample are highly desirable. In order to achieve it, an equipment to externally induce the strain to the sample was developed, using the four-point bending mechanical principle, illustrated in fig. 4 [9].

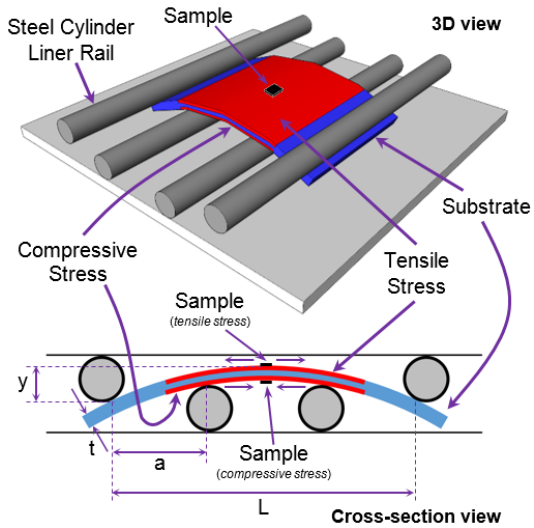

Fig. 4. *3D and cross-section view of the four-point bending mechanical principle.*

In fig. 5 are presented images of the mechanical bending setup developed and placed in the probe station that will be used in future works to characterize the samples experimentally.

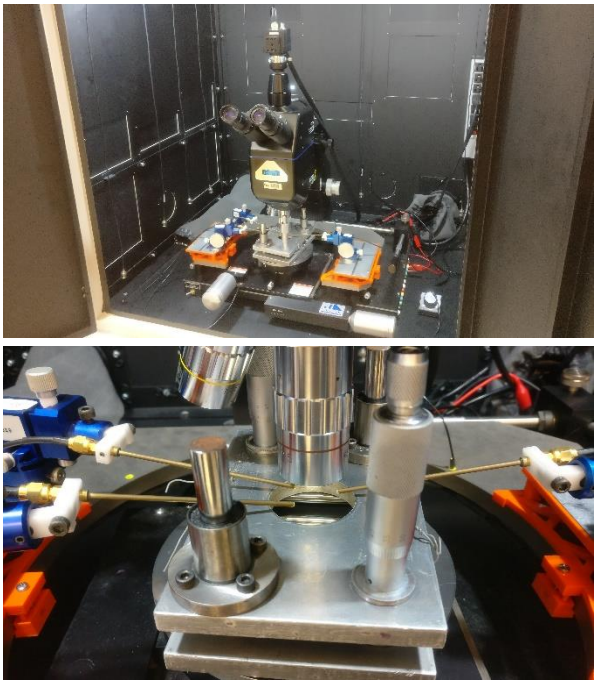

Fig. 5*. Proposed mechanical bending setup for experimental characterization.*

7. Conclusions

The response of the PIN photodiode to the light incidence in reverse polarization was verified with the increase in the electric current with different wavelengths, justifying the optical application of the device. The application of mechanical stress through numerical simulations returned the change in electrical current by changing the bandgap and the rate of scattering carriers, altering the electrical current in the reverse bias condition.

Acknowledgments

The authors thank CAPES for financial support.

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Analysis of wire bonding and tape pull-test on electrolytic gold-thin-films to use as interconnection in MCM-D packaging.

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1. Abstract

Multichip Module (MCM) packaging provides one means of achieving high chip densities and shorter interconnection lengths. In terms of electrical performance, MCM also provides lower power supply inductance, lower capacitance loading, less cross talk, and lower off-chip driver power. Die attach and bonding technology used in this kind of integration are mainly: Wire-Bond, Tape Automated Bonding (TAB) or Flip-Chip, where high-density interconnects are determinants for the proper functioning of the device. The present work reports the analysis of wire bonding and pull-test made on gold (Au) electrolytic-thin-films, destined essentially to interconnect the different circuit levels on the MCM. The results evidenced a high dependency between the thicknesses of the Au films and the quality of welding points, being obtained the best result for Au films with thickness of 3 μm.

2. Introduction

Classic thin-film hybrid technology (MCM-D) is an example of a technique that fall into MCM packaging. This technology is based on one thin gold signal layer on top of an alumina (Al_2O_3) substrate. Crossovers are made by wire bonding. The backside of the substrate can be gold coated for the use as a ground plane [1]. Specifically in the technological process of MCM-D production proposed by our research group (Electronic Packaging Research Group, Renate Archer Center for Information Technology (NEE-CTI)) Al_2O_3 (96% and 2.5 cm × 2.5 cm) is used as substrates and polymer benzocyclobutene (BCB) photosensitive as insulator and dielectric in the capacitive elements of the device. The interconnections and the passive elements are formed by several sequences of deposited metallic thin films and defined by photolithography processes [2]. Therefore, the good quality of the welding points is crucial in order to ensure a good interconnection between the components and levels that constitute the MCM-D integration and with this, the good performance of the device.

In this context, the present work propose the study of wire bonding and pull-test in gold (Au) films for interconnections, using wires of aluminum (Al) and Au with thicknesses of 31 μm and 17 μm respectively.

3. Experimental Details

For this study, a group of samples were fabricated following the sequences shown in Fig. 1.

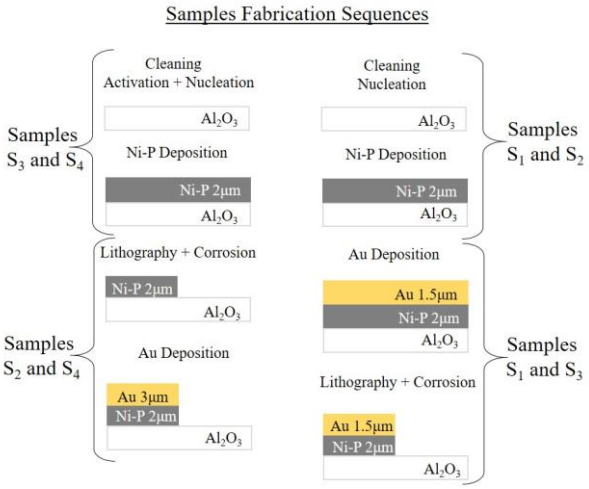


Fig.1. *The samples fabrication sequences used in this study.*

As can be seem in Fig. 1, samples 1 and 2 (S_1 and S_2 respectively) were made using conventional deposition of electrolytic Au-films, meanwhile samples 3 and 4 (S_3 and S_4 respectively) were manufacturing using an activation step (HF/NH_4F) before the Au deposition. In addition, the thickness of S_1 and S_3 is 1.5 μm whereas that S_2 and S_4 have 3 μm. Therefore, in this study we focus in the influence that the thickness and the activation step used in the fabrication process of the samples, have in the quality of the welding points intended for interconnections in the integration technology MCM-D proposed by our research group [2]. To characterize the bond quality and strength of the Au and Al wires on the Au thin films, method 2011.8 from MIL-STD-883H [3] was applied.

4. Results and Discussion

From the wire bonding test results it was observed that samples S_1 and S_3 did not supported the wire bonding process, due to detachment of the Au film during the process, whereas the Ni-P underlayer remains intact. On the other hand, the samples S_2 and S_4 reported a perfect adhesion of the welding points for both the Au

wires and the Al wires. Fig 2 shows the results of the latter's (S_2 and S_4)

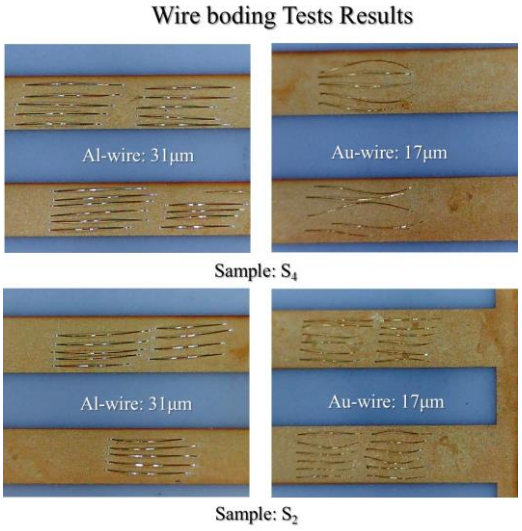
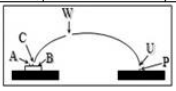


Fig.2. *Wire bonding Tests Results for samples S_4 (Up) and S_2 (down) for wires of Al and Au.*

Destructive pull-test evaluation was performed on the wires bonded onto samples S_2 and S_4 that were the only ones that withstood the welding. Results are presented on Table I.

Table I. *Pull-test results for Al (31 µm) and Au (17 µm) wires for samples S_2 and S_4.*

Wires No.	Pull-Test Results							
	Al wire				Au wire			
	S_2		S_4		S_2		S_4	
	GR	COD	GR	COD	GR	COD	GR	COD
1	7	C	6	C	2	U	2.5	C
2	8	U	7.2	U	2.5	C	2.5	C
3	8	C	7	U	2	C	25	C
4	8.2	C	7	C	3	C	2.5	C
5	6	C	6.2	C	2	C	2	C
6	5.5	U	6.5	C	2	C	3	C
7	6.2	C	8	C	2	C	2	C
8	7	C	7	C	2	C	2.5	C
9	6	C	5.5	C	2.5	C	2	C
10	8	C	7	U	3	C	2	C
11	5.5	C	8	C	2.2	C	3	C
12	5.5	C	6.8	C	2	C	2	C
13	7	U	7	C	2	C	3	C
14	6.5	C	8	C	2	C	2	C
15	6.5	C			3	C		
SUM	100.9		97.2		34.2		33.5	
HV	8.2		8		3		3	
LV	5.7		5.5		2		2	
AVE	**6.7**		**6.9**		**2.3**		**2.4**	



HV: Higher value
LV: Low value
AVE: Average
GR: Grams

Code (COD)

A: Raised matrix terminal
B: Raised matrix solder
C: Broken wire at matrix junction
U: Broken wire at box junction
P: Raised box solder
W: Broken wire on the meb

As expected for a good wire bonding, most of the breakages happened on the border of the bonding (COD = C or U), with no detachment observed from the pull (COD = A or B). This demonstrates that the Au films deposited have enough adherence to receive and maintain the interconnections. Quantitatively, we observed that the force required for breaking the wire (see line AVE on Table I) is above the specifications established according to the MIL-STD-883H standard [3]. These values are 2.0 grams (force) for Au wire with 17 µm of diameter and 3.0 grams (force) for Al wire with 31 µm of diameter. Fig. 3 illustrates some results of Table I for sample S_2.

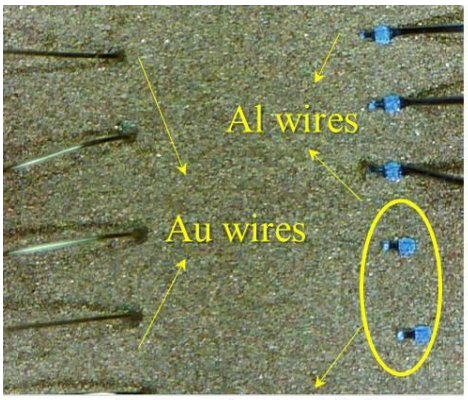


Fig.3. *Pull-test image for sample S_2.*

5. Conclusions

From the results obtained in this study it could be conclude that, in the evaluation of the quality of adherence and resistance of the welding points, the parameter that has the greatest influence is the thickness of the Au films. The influence of the activation or not of the Al_2O_3 substrates before the deposition sequences is practically imperceptible. The best results were observed for the samples S_2 and S_4 with Au thickness of 3 µm. Both minimum values reported by pull-test for these samples (S_2 and S_4), are above the specs established in the MIL-STD-883H standard [3].

Acknowledgments

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A Low-Cost Pre-Amplifier for Current Measurement in Sub-nA Range

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1. Abstract

This work presents a low-cost circuit that enables the measurement of electrical currents below the nA range. The circuit presents an output current that is an amplified version of the unknown current. Simulations using MOSFETS and bipolar junction transistors showed that the current gain can be adjusted over five decades with high linearity. The relation between the measured current and the unknown current has also good linearity for five decades. The circuit is intended to be used by the CITAR (acronym in Portuguese for Radiation Tolerant Integrated Circuits) project members.

2. Introduction

CITAR (acronym in Portuguese to Radiation Tolerant Integrated Circuits) is a project involving many Brazilian research institutions and universities in the research of radiation effects on semiconductors and the design of chips using the Radiation Hardness by Design (RHBD) approach. Among the results of this project, devices with some news geometries, e.g., Diamond and OCTO MOSFETs were proposed and proved to be more tolerant to radiation than their conventional counterparts [1], [2].

The characterization of such devices after being submitted to radiation is made measuring the drain-source current (I_{DS}) as a function of the gate-source voltage (V_{GS}). The current varies by several orders of magnitude, since the device should be characterized even in subthreshold region, where the current is limited to the charges diffusion in the channel.

To perform the electrical characterization of semiconductor devices in their sublimation region, precision SMU (Source and Measurement Unit)-type instrumentation is required to measure electrical currents smaller than 1 nA, but these SMUs are very expensive.

This work proposes a low-cost circuit which aims to extend the current limit down to pA range, thus solving this kind of limitation in the instrumentation. The circuit is based on the exponential relationship between currents and voltages of MOSFETs in weak inversion and bipolar junction transistors (BJTs).

Section 3 presents the circuit and explains the working principles for MOSFETs and BJTs. Section 4 brings simulated results using devices from XFAB XC06 technology. Conclusions and future works are presented in Section 6.

3. The Current Measurement Circuit

The measurement method is based on the principle of log converters. A circuit for measuring currents higher than 10 nA using this principle is presented in [3]. The proposed circuit is illustrated in Fig. 1. Both transistors (M_0 and M_1) are biased at constant V_{DS}, in order to reduce the variation of the leakage currents [4]. M_0 and M_1 are biased in the weak inversion region and in this case their currents are given respectively by [5]:

$$I_{DS0}=I_0 exp[V_{GS0}/(nV_T)]\{1- exp[V_{DS}/(nV_T)]\}, \quad (1)$$

$$I_{DS1}=I_0 exp[V_{GS1}/(nV_T)]\{1- exp[V_{DS}/(nV_T)]\}, \quad (2)$$

where V_T is the thermodynamic voltage, V_{GS0} and V_{GS1} are the gate-source voltages of M_0 and M_1 respectively, I_0 and n are related to geometry and technological parameters of the transistors [5] and V_{DS} is the drain-source voltage. If V_{DS} is greater than 200 mV, the last exponential term in (1) and (2) can be despised.

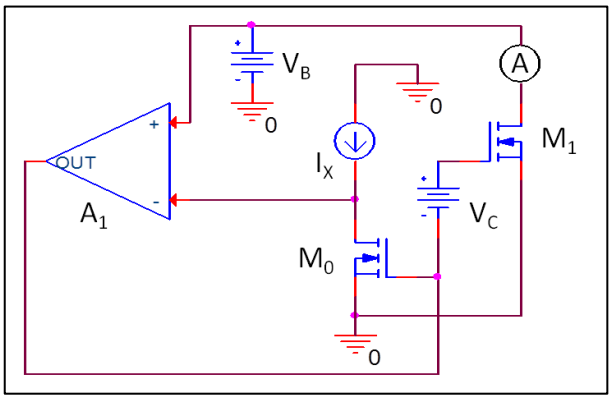

Fig.1. *The current measurement circuit.*

The opamp adjusts V_{GS0} through feedback in order $I_{DS0}=I_X$ (the unknown current). V_{GS1} is given by

$$V_{GS1}=V_{GS0}+V_C. \quad (3)$$

Using (1), (2) and (3) and neglecting the exponential terms involving V_{DS}, one can prove that I_{DS1} is given by

$$I_{DS1}=I_X exp[V_C/(nV_T)]. \quad (4)$$

Then the current to be read is an amplified version of the unknown current. The relation between voltage and current is exponential, thus a small control voltage (V_C) can represent a great amplification factor.

A similar reasoning is made when M_0 and M_1 are replaced by BJTs. In this case the collector current I_C is given by the following approximate equation when V_{BE} (the base-emitter voltage) is higher than 100 mV [6]:

$$I_C = I_S exp(V_{BE}/V_T), \quad (5)$$

where I_S is the reverse saturation current of the transistor. Due to the similarity between (1) or (2) and (5), it is evident that (4) applies for the circuit with BJTs making n equal to 1.

4. Simulated Results

The circuit was simulated using MOSFETs nmos4 and BJTs qnve from XFAB XC06 (0.6 µm Bulk CMOS) technology using Cadence Virtuoso®. The size of the MOS transistors was adjusted in order the leakage current compensates the nonlinearity of the controlled current below 10 pA. The effective area of the MOSFET is 2816 µm (width) x 1.0 µm (length). The area of the BJTs is 40.8 µm x 31.6 µm.

Fig. 2 shows I_{DS1} as a function of I_X when V_C is set to 123 mV for BJTs and 178 mV for MOSFETs. This way the current gain is 100 for both devices. Bias voltage V_B is 250 mV.

The circuit shows good linearity for five decades, with a slightly inferior performance for the case with BJTs below 10 pA.

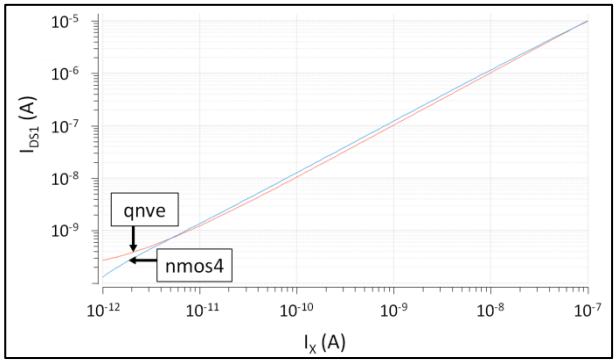

Fig.2. *I_{DS1} as a function of 1_X. Current gain is 100.*

I_{DS1} was measured as a function of V_C, with I_X fixed at 100 pA. Results are shown in Fig. 3. Current could be amplified for over five decades with very good linearity. The difference in the lines inclination is due to different values of n (1.00 for BJTs and 1.45 for MOSFETs).

4. Conclusions and Future Works

The gain of the circuit could be adjusted up to five orders of magnitude, enabling that the instrumentation type SMU, e.g., a PXI-4132 from National Instruments used by CITAR participants could be used to measure currents below 1 nA. The current gain and the relation between the output current and the control voltage show very good linearity. The circuit using MOSFETs with optimum size presented a slightly superior result than that when it uses BJTs, especially for currents below 10 pA.

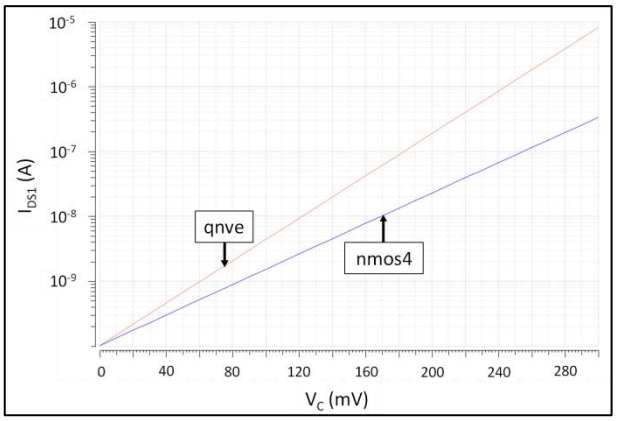

Fig.3. *I_{DS1} as a function of V_C. I_X is fixed at 100 pA.*

However the BJTs size is less than half of the MOSFETs size.

Real leakage currents are quite difficult to predict by simulation. Thus the validation of the concept only will be possible with the fabrication of the chip when the effects of leakage currents in the performance of the circuit will be evaluated.

Another point for future work is making V_C as a function of the temperature. Despite the circuit is thought to be used in lab environment, the exponential coefficient of the current gain involves V_T, which depends of the temperature. This way, even fractions of Kelvin variations may result in a significant impact in the current gain.

Acknowledgments

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Electric Characterization of Gold Stud Bumps used in Flip Chip Technology

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1. Abstract

Daisy Chain structures were used to measure contact resistance of Gold (Au) stud bumps. Au stud bumps were fabricated over the chip using a modified wire bonding process. Then the chip was flipped onto an Au covered Alumina substrate using a thermocompression/sonic process. The electric resistance of all structures were measured as a way to calculate the contact resistance from the Au stud bump.

2. Introduction

Flip chip packaging involves applying soldered bumps on the top side of a fabricated wafer. The integrated circuit can then be flipped and aligned with grooves on an external circuit to enable the necessary connections. This form of packaging occupies less space in products and offers higher input/output rates because the whole surface area of the chip can be used for interconnection rather than around the periphery of the chip going beyond the number of package pins required by the Rent´s rule [1]. This 2D-array structure can save chip space and reduce the footprint of the chip on the substrate.

Flip chip assembly offers many advantages, mainly improved electrical performance. The small bumps of flip chip interconnection provide short electrical paths, which yield excellent electrical properties with low capacitance, inductance, and resistance. This results in greatly improved high-frequency performance compared to other interconnection methods such as chip-and-wire.

Existing 2-D integrated circuit (2.0DIC) flip-chip and wafer-level packaging technologies have shown solid growth over the past five years [2] and are used in a number of mainstream applications predominantly in high-end smartphones and many wireless device suppliers are expanding their use of flip chip technology to high-end ICs. For instance, 75% of new ASIC designs are now in the flip chip format, and this percentage is increasing. Flip chip is used to allow advanced packaging, such as:

– LG Innotek developed flip-chip LED package allowing stable 220lm/W efficiency.

– Intel has unveiled a superconducting quantum test chip with 49 qubits, to enable quantum computing that begins to exceed the practical limits of modern classical computers through flip chip technology [2].

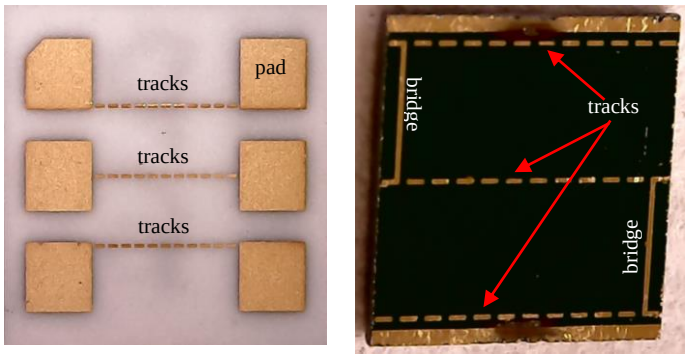
The global flip chip technology market is segmented on the basis of wafer bumping process, packaging technology, packaging type, product, application, and region. On the basis of the wafer bumping process, the segment is further classified into copper (CU) pillar, lead-free, Tin-lead eutectic solder and gold stud plated solder. On the basis of the packaging technology, the market is further classified into 2D, 2.5D, and 3D packaging technology. On the basis of the packaging type, the market is further classified into FC BGA (Flip Chip Ball Grid Array), FC PGA (Flip Chip Pin Grid Array), FC LGA (Flip Chip Land Grid Array), FC QFN (Flip Chip Quad Flat No-Lead), FC SIP (Flip Chip System-In-Package), and FC CSP (Flip Chip-Chip-Scale Package). On the basis of the product the segment is further classified into LED, CMOS image sensor, CPU, RF, Analog, Mixed Signal, and Power IC, SoC and others. Flip chip technology is widely used in many areas such as consumer electronics, automotive, telecommunications, industrial, medical devices, military and aerospace and others.[2-6]

The global flip chip technology market is estimated to grow at 8.29% CAGR through the forecast period (from 2018-2023) [2].

3. Experimental Procedure

To measure the Au stud bumps contact resistance in this project, daisy chains, that is, interconnection structures containing Au tracks and pads for electrical measurements were built. Electrolitic Au was deposited onto 25,4 x 25,4mm Alumina to be used as substrate while sputtered Au onto 2 inch oxidized silicon wafer serve as chip to be flipped. These pieces were printed and etched to form 300x100um tracks and diced to provide 10x10mm substrates (Fig. 1a) and 5x5 mm chips (Fig. 1b) for the flip chip tests.

Four Au stud bumps were made on the extremes of the chip bridges (long tracks in the chip) using a modified wire bonding process [3]. The chip was then flipped, aligned and bonded onto the substrate using the Eagle 860 Omni Bonder (Semiconductor Equipment Corp.) in the thermocompression/sonic process (Fig. 2a and 2.b).



(a) (b)

Fig. 1. *(a) Alumina substrate and (b) Chip*

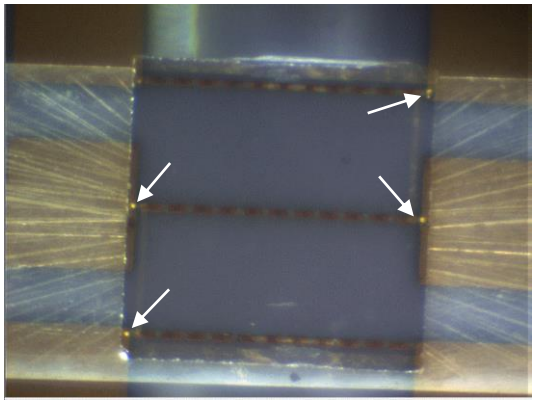


Fig. 2. *Substrate and Chip alignment using the Eagle 860 Omni Bonder equipment before flipping. White arrows indicate the Au stud bumps.*

4. Results and Discussion

Table 1 below shows the bonding parameters used in this experiment [3].

Table 1. *Parameters for Flip Chip using Au stud bumps on the Eagle 860 Omni Bonder equipment*

ULTRASONIC PARAMETERS (SERVO MODE)			MACRO PARAMETERS			
START LOAD (g)	ULTRASONIC TIME (ms)	ULTRASONIC POWER (EU)	STAGE TEMPERATURE (° C)	PICK LOAD (g)	BOND LOAD (g)	BOND TIME (s)
250	1500	2500	120	10	400	5

The electric resistance (mΩ) for the tracks and bridges on the chip and substrate before bonding and for the flip chip set after bonding were measured using the Agilent Technologies B 1500A Semiconductor Device Analyzer (4 point probe configuration). The difference in resistance before and after Flip Chip are due to the contact resistance from the two Au stud bumps formed on the edge of the bridges (Fig. 2). Table 2 shows the final value per Au stud bump in each bridge.

The large spread on the contact resistance values is due to the tail formed during the bumping process, which leads to non-uniform bump heights and thus, impacts negatively the interconnection.

Table 2. *Resistance and Contact resistance in (mΩ) for the Au stud bump characterization*
(r = right bridge; l= left bridge)

Sample	Before flip chip	After flip chip	Contact resistance
1-r	6,70	8,39	0,85
1-l	6,65	7,90	0,63
2-r	5,99	6,30	0,16
2-l	5,66	open	open
3-r	6,90	open	open
3-l	6,93	7,33	0,20
4-r	6,69	6,90	0,11
4-l	6,65	open	open

5. Conclusions

Results show the viability of the flip chip and MCM (Au deposition) processes available at the Electronic Packaging Research Group from CTI Renato Archer (NEE-CTI). Studies will continue in order to obtain a better control and reproducibility of the Au stud bumps for a more uniform contact resistance distribution in the future tests with real circuits and devices.

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Back Biasing Vertically Stacked Nanowires SOI p-type MOSFETs

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1. Abstract

The aim of this work is to present an analysis of vertically stacked p-MOSFET nanowires under different back bias conditions. Back bias is used to explore the electrical properties of advanced stacked NWs in order to dissociate both Ω-shaped bottom and Gate-All-Around top channel conductions. The evaluation is carried out through tridimensional numerical simulations and experimental measurements. Drain current, transconductance, holes density, threshold voltage and low field mobility are the figures of merit.

2. Introduction

Nanowires (NWs) MOSFETs are advanced multiple gate structures characterized by being stripes of semiconductor material with close dimensions for both fin width (W_{FIN}) and silicon thickness (H_{FIN}), in the order of 10 nanometers, surrounded by gate contact [1], [2]. Due to improved electrostatic control of the charges in the channel region and, therefore, reduced short channel effects, the NW is one of the most promising devices for future technological nodes that would allow the continuity of the CMOS roadmap [2].

Recently, Fully-Depleted (FD) Silicon-On-Insulator (SOI) process technology has been adapted to vertically stack two levels of NWs [3]–[5]. The resulted structure, called vertically stacked NW, presents a Ω-shaped bottom level and a top Gate-All-Around (GAA) level [4]. Stacked NWs enhances the overall drive current due to larger effective channel width, which is approximately proportional to the number of stacked levels [6].

In this work, each of the two levels that compose the vertically stacked structure is evaluated individually by applying different back bias (V_B). The channels dissociation brings valuable information for further technology optimization. Tridimensional numerical simulations are used to understand the physics of vertically stacked NWs and, finally, the methodology proposed in [7] is used to extract the low field mobility of each level.

3. Devices characteristics

The studied transistors are undoped p-type silicon nanowires MOSFETs with two staked levels. Silicon thickness is equal to 10nm and W_{FIN} is equal to 15nm. The geometrical parameters W_{FIN} and H_{FIN} are the same for both top and bottom wires. The buried oxide thickness is 145nm and the channel length is equal to 100nm.

Fig. 1 shows the studied structures, where (a) and (b) indicates, respectively, the longitudinal section and cross-section of the simulated stacked NWs. The physical characteristics of the transistors have been simulated in order to reproduce the physical devices fabricated in [4], whose longitudinal section and cross-section are represented in Fig.1 (c) and (d), respectively. Once the fabrication process starts from FD SOI wafers, the bottom level is Ω shaped, while the top level is GAA.

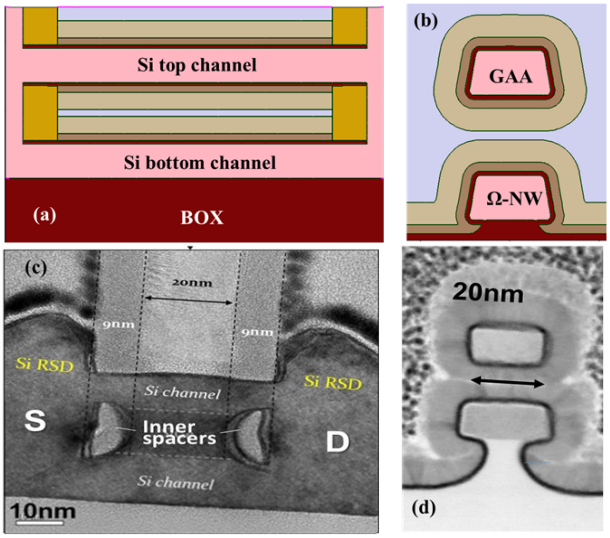

Fig.1. *Simulated and measured stacked NW longitudinal section (a) and (c) and cross-section (b) and (d).*

4. Channels conduction dissociation

Fig. 2 shows simulated results for drain current (a) and transconductance (b) of the stacked NW structure (lines), the bottom Ω-gate level (closed symbols) and the top GAA level (open symbols), varying V_B. Sentaurus Device Simulator, from Synopsys, has been chosen to perform all the tridimensional numerical simulations [8]. It is observed that the stacked NW changes with V_B variation, due to the Ω-gate level dependence on V_B. As the GAA is surrounded by the front gate, the top level is V_B independent and its I-V characteristics do not change with V_B. The back gate induces significant control over the bottom level, through the base of the Ω shape, so the drain current of the bottom Ω-gate NW shifts to the left with V_B increase, indicating threshold voltage decrease. Moreover, Fig.2 (b) shows that the maximum

transconductance of the Ω-gate NW reduces with V_B increase, indicating mobility degradation.

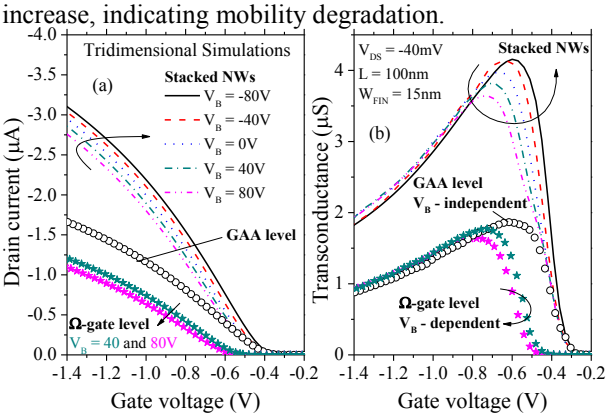

Fig.2. *Drain current (a) and transconductance (b) as a function of gate voltage for simulated stacked, GAA and Ω-gate p-NWs with W_{FIN} =15nm, L = 100nm, at V_{DS} = -40mV.*

From the holes density distribution in Fig. 3, it is confirmed the immunity of the top GAA level to V_B change, once for both V_B = -80V and 80V results are the same. On the other hand, the bottom Ω-gate NW shows significant V_B dependence. At V_B = 80V, the bottom level is in off-state, the high positive V_B pushes the holes towards the first interface and the channel is mainly depleted. At V_B = -80V, the bottom level is conducting and the high negative V_B pulls the holes across the back interface. The back bias modulates the inversion channel density, pushing and pulling carriers along the silicon thickness, changing their mobility.

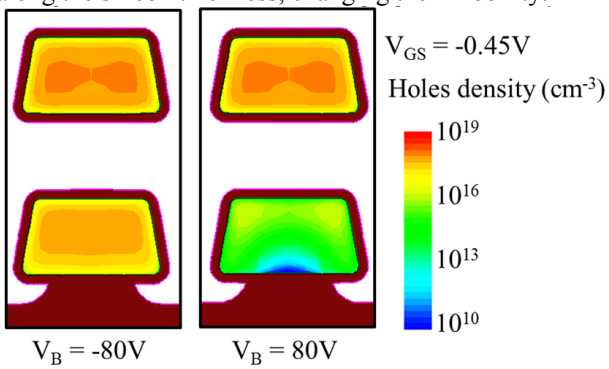

Fig.3. *Holes density distribution along the fin width of stacked p-NW with W_{FIN} = 15nm at V_B = -80V (a) and 80V (b) and V_{GS} = -0.45V.*

Following the idea represented in Fig. 3, where V_B can be used to turn the bottom level off while the top level is conducting, it is possible to promote the electrical characterization individually of each level. Applying the procedure proposed in [7], Fig. 4 shows experimental results for the threshold voltage (a) and low field mobility (b) of stacked NWs at V_{DS} = -40mV. Top and bottom levels were dissociated by using back bias and Y-function method [7], [9]. Closed symbol indicates parameters dependence of Ω-gate level on V_B, while the open symbol shows constant behavior for the top GAA level. As predicted by simulations in Fig. 2, the low field mobility of the bottom level reduces with V_B increase, which is mainly due to the position of the inversion channel, as discussed in Fig. 3.

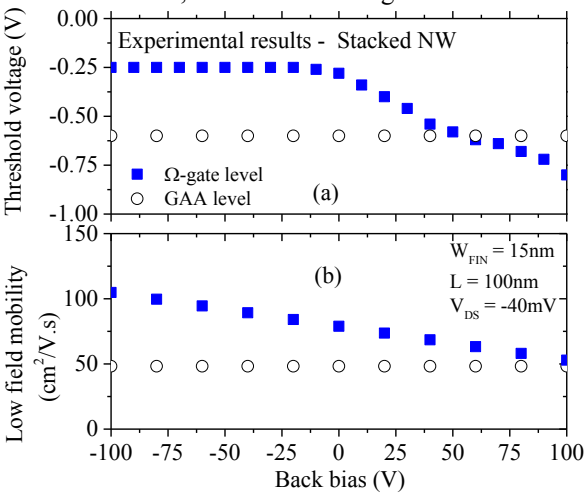

Fig.4. *Experimental results for threshold voltage (a) and low field mobility (b) of bottom and top level of stacked p-NW with W_{FIN} = 15nm and L = 100nm, at V_{DS} = -40mV.*

5. Conclusions

This work presented an analysis of back bias variation on two levels vertically stacked nanowires p-type MOSFETs fabricated from FD SOI wafers. Back bias has shown to be a useful tool to dissociate the two channels conduction for mobility characterization.

It has been observed that the top GAA NW presents degraded threshold voltage and mobility in comparison to the bottom Ω-gate NW, indicating the need of technological optimization for better overall performance of the stacked structure.

Acknowledgments

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Single-Event Upset in PIN-SOI diodes due to heavy-ion incidence

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1. Abstract

PIN diodes are devices that have wide applicability in several segments, such as ultraviolet rays sensing, optical communication, gases detection and classification and space observation. The basic difference between PIN and PN diodes is the presence of an intrinsic region (P^-, weakly doped) between anode (P^+) and cathode (N^+) regions. The main reason that justify all these applications of the PIN diodes is its satisfactory response to radiation events, one time these devices can electrically react to radiation impacts before the recombination of the generated carriers. The devices used, presented in Fig. 1, are lateral PIN diodes based on SOI (Silicon-On-Insulator) technology, in order to minimize effects of parasitic capacitances [1]. Experimental data obtained by laboratory measurements on the devices provided by UCL (*Université Catholique de Louvain*) was used to adjust the models implemented in the numerical simulator (Sentaurus, by Synopsys [2]) that are used to evaluate the radiation analysis for heavy-ion particles.

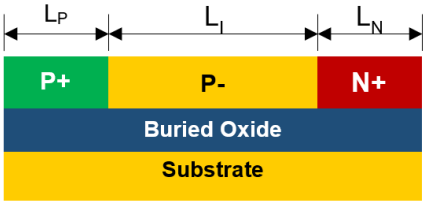

Fig.1. *Schematic representation of a lateral PIN-SOI diode*

2. PIN-SOI's behavior before radiation strike

In way to identify the influence of the radiation incidence on the PIN-SOI diodes, it was necessary to know how they operate in dark situation (absence of radiation incidence). In this situation, the current levels of the devices depend only of the bias that polarizes them. Six devices were simulated in this condition, each one with a different intrinsic region length (L_I), polarized with the cathode and the substrate on the reference bias (0V), the anode being excited by a bias ramp (V_{an}), starting on -2.0V and reaching +2.0V, and the current values (I_{cat}) were monitored, according to Fig. 2. Vary the intrinsic region length just modify the direct current levels, while the reverse current remains at the same level, once it depends fundamentally of the electric field. Then, the effect of increasing the distance between the devices' terminals (caused by increasing the intrinsic region length) on the direct current is negligible.

When PIN diodes are used as photodetectors, they are polarized reversely, as this configuration provides lower dark current levels and makes that the current generated by the Single-Event Upset (SEU) can be distinguished more clearly [2].

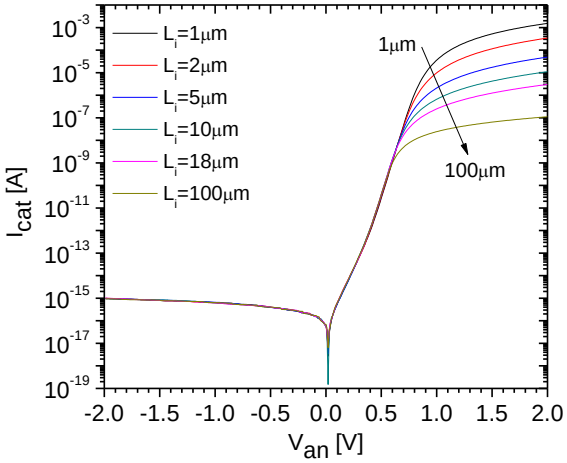

Fig.2. *I_{cat} x V_{an} for different L_I without radiation incidence*

3. Heavy-ion strike: the Single-Event Upset (SEU) phenomenon

When a heavy-ion strikes a reversed biased junction, the depleted region is distorted according to the particle's path, creating a kind of "funnel". This trajectory leaves electrons-holes pairs as a trace, which compose a photogenerated current in the device [1][3]. To investigate this situation, different positions of the 1μm device were struck by heavy-ion, like shows Fig. 3. The collision of the heavy-ion with the PIN-SOI occurs at the instant of 1ns and the linear energy transfer (LET) of the heavy-ion (sodium was used) is 1MeV.cm²/mg. As reference, the LET of 1MeV.cm²/mg is equal to a charge deposition of 0.01pC/μm, based on the energy of 3.6eV to generate an electron-hole pair in silicon [3]. Cathode and substrate contacts are fixed on the reference bias (0V).

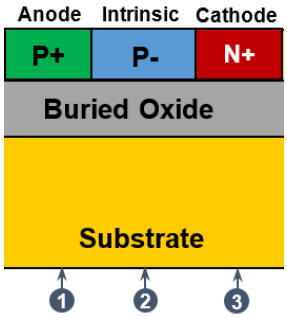

Fig.3. *Positions which heavy-ion struck the PIN-SOI diode*

First, the heavy-ion strikes, one at a time, the cathode and anode regions (Fig. 4). It's possible to notice that the

peak current generated when the particle struck the cathode region (Pos. 3) is almost two times greater than the peak observed at the anode region (Pos. 1). The main concept that explain this result is that the photogenerated electron-hole pairs migrate to the terminal of lower potential (once they are guided by the electric field) and that these pairs have a finite lifetime on the silicon structure before they are recombined [4]. It means that once the cathode is grounded, the carriers generated by colliding the cathode region must displace a path too lower than the carriers generated at the anode region, fact that increases the chance of the carriers being effectively detected as current before recombined. It's also possible to see at Fig. 4 that the curve of the position 3 (cathode) has a most concentrated shape than position 1 (anode). Once the carriers generated at cathode region are detected too fast, only the drift current component (high magnitude, low duration) is sufficient to drive the carriers. For the generation at anode's region, the drift current displaces the first carriers generated, but there remains carriers that are driven by the diffusion current (low magnitude, high duration).

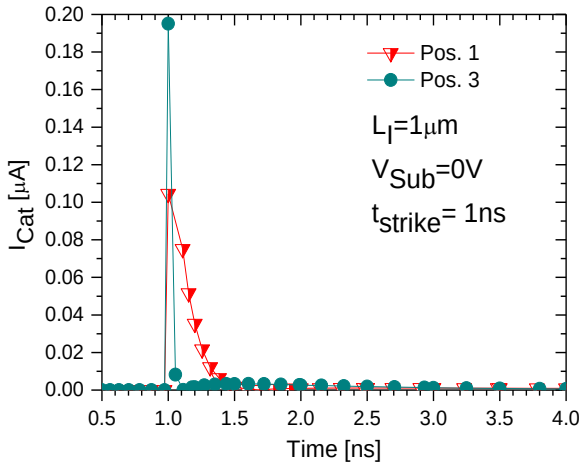

Fig.4. *Heavy-ion hitting cathode and anode regions*

In Fig. 5, the heavy-ion struck the intrinsic region of the 1μm PIN-SOI device. The maximum photogenerated current in this situation reached almost 17μA, which is about 85 times greater than the peak current generated at cathode region (near 0.2 μA). However, the level of current generated hitting the intrinsic region is too much susceptible to the increase of the intrinsic length (L_I), showing that the absence of minority carriers is the main factor to detect the generated carriers only if the distance to the reference terminal is maintained small. Fig. 6 shows the effect on the generated current caused by increase the intrinsic region length. It's possible to see that just changing L_I to 2μm makes the current reaches just 2μA. For the device of L_I=5μm, the current levels are smaller than 0.5μA. To ensure the detection of photogenerated current, the L_I dimension can be increased up to the diffusion length of the device's technology [5].

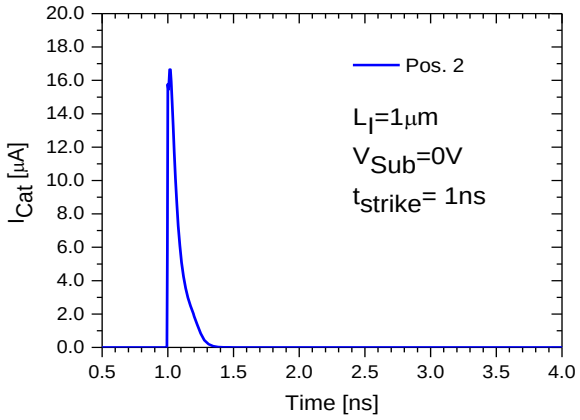

Fig.5. *Heavy-ion hitting the intrinsic region of the 1μm device*

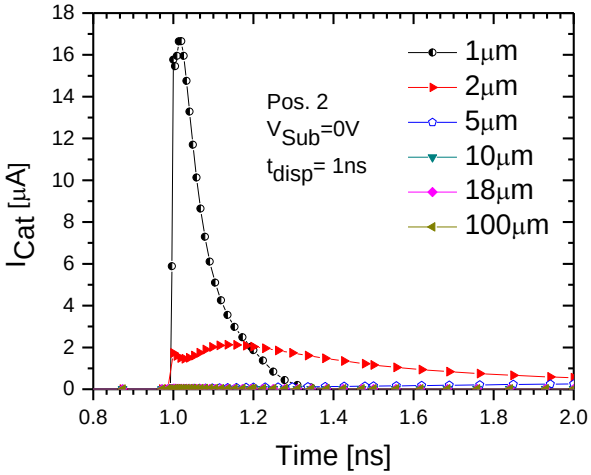

Fig.6. *SEU generated current with the intrinsic region length variation*

4. Conclusions

Although it is interesting to increase the intrinsic region area in order to increase the chance of a particle to hit the device on a region of high yield (cathode or intrinsic), it was shown that it is heavily contrasted by the recombination rate factor. This situation must be balanced according to the photodetectors' project, in order to ensure the detection of radiation presence and to clearly distinguish it levels. It is also possible to expand this analysis to other heavy-ions and to design a particle detector, once the electric current is a function of the incident position and the particle's LET.

Acknowledgments

The authors would like to thank CAPES for the financial support and UCL for the provided devices.

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Strained Silicon Nanowire without External Mechanical Actuators

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1. Abstract

Mechanically stressed semiconductors present several physical properties related to changes in their electrical (enhancement of carrier mobility), thermal and optical properties due to modifications in the material band diagram. Moreover, the fabrication techniques utilized to create stressed structures are of vital importance, as it presents a limiting factor to achieve high stress, stress uniformity, stress type (uniaxial, biaxial, compressive, tensile), as well as the need to use external actuators among other factors. In this sense, it is proposed a top-down approach to obtain suspended silicon nanowires with uniaxial tensile strain, without external mechanical actuators and patterned in e-beam lithography. This approach consists in minimization of elastic strain energy of a pre-strained substrate by removal of a sacrifice layer. The strain characterization, by Raman spectroscopy, indicates nanowires with a high tensile strain of ~ 3.7%. This method can be an alternative for electrical carrier mobility enhancement, extending microelectronics roadmap.

2. Introduction

Electrical improvement of microelectronics devices is essential for switching velocity optimization, and power consumption reduction. In this way, the strain is considered a powerful tool for industry extending CMOS roadmap [1].

An alternative, proposed by Reference [2], is the patterning of a suspended nanowire configuration for strain enhancement. This method consists in using a pre-strained layer with a sacrificial layer. The release of the nanobridge structure when removing the sacrificial layer changes the system configuration, accumulating the strain at the nanowire constriction with a reduced area [3].

In this work, this approach was performed with a sSOI substrate (strained Silicon On Insulator) composed of a thin film (15nm) of biaxially strained silicon (0.8% tensile strain) on a 145nm silicon dioxide (sacrificial layer). The final strain in the nanowire was measured by Raman spectroscopy.

3. Results and Discussion

A. Nanofabrication process

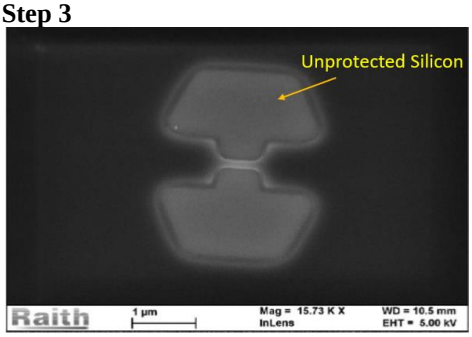
The fabrication process has the following steps:

1) Organic cleaning of the sSOI substrates;
2) Electron resist deposition and spinning;
3) Ebeam lithography for pattern transfer;
4) Reactive Ion Etching (RIE) of unprotected silicon;
5) Wet etching of sacrificial oxide for suspension.

Fig. 1 shows the results after steps 3 (Fig. 1.a) and 4 (Fig. 1.b). The unprotected silicon region (Fig. 1.a) was dry etched in step 4 anisotropically. As a result, a hole is opened for the wet etching process (Step 5). At the final stage, an HF buffer (7%) is used to etch the silicon dioxide under the bridge to obtain a suspended bridge. This etching process is selective, thus maintaining silicon thin film.

The final structure is in Fig. 2. With a scanning electron microcospe (SEM) image is possible to see the underetching region that results from step 5.

a) Step 3



b) Step 4

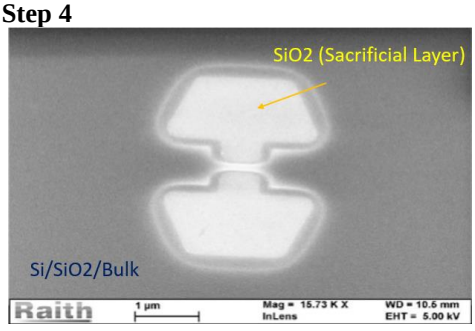


***Fig.1**. a) Ebeam patterning transfer of the nanobridge (Step 3) b) RIE of unprotected silicon.*

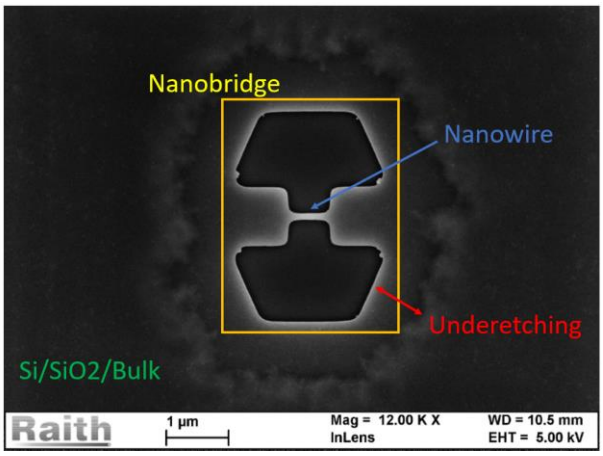


Fig.2. *Nanobridge final structure.*

B. Strain Characterization by Raman Spectroscopy

The Raman measurement using a laser wavelength of 514nm, and focused at the center of the strained nanowire is shown in Fig. 3.

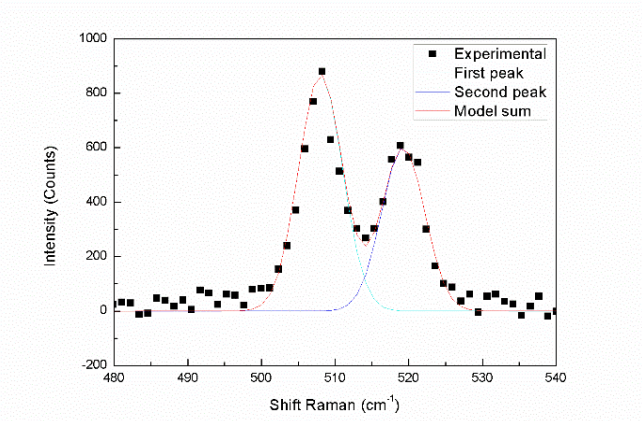


Fig.3. *Raman spectrum of the silicon nanowire center. The fitting of the peaks were performed with the software Fityk* [4].

The first peak, at ~ 520cm^{-1}, is related to silicon bulk substrate signal, due to penetration of the laser in its current wavelength. The second peak, at ~ 508, is the signal from the tensile strained nanowire.

The strain at the center of the nanowire is determined by the semi-empirical equation for uniaxially strained silicon [5]:

$$\Delta\omega = -3.27\text{cm}^{-1} \times \varepsilon_{xx} \quad (1)$$

Where:

$\Delta\omega$: Raman shift between the reference peak of a regular silicon substrate (~ 520 cm^{-1}) and the measured peak at the nanobridge center (~ 508 cm^{-1}).

ε_{xx}: Strain at the nanobridge center in percentage (%)

Using equation (1), a strain of ~ 3.7% is achieved.

4. Conclusions

Suspended nanobridges fabricated at the sSOI wafer, with a conventional top-down process, presented high uniaxial tensile strain of ~ 3.7% without the use of external actuators.

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The authors thank the financial support by FAPESP and CNPq.

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Silicon channel thinning using NH_4OH wet etching

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1. Abstract

Junctionless-FET (JL-FET) devices were fabricated on SOI wafers using anisotropic silicon etching in a NH_4OH solution. Silicon Oxynitride was grown using O_2/N_2 Electron-Cyclotron-Resonance (ECR) plasma as gate dielectric, and Titanium Nitrate was deposited using reactive sputtering as gate metal. The structure was characterized using SEM imaging and electrical measurements. The final Si channel thickness obtained was 65nm and the electrical behaviour of the device was as expected.

2. Introduction

Junctionless-Field-Effect-Transistors (JL-FET) devices were first introduced as an alternative to traditional enhancement type MOSFET devices, especially because the JL-FET doesn't require expensive ultra-fast thermal annealing techniques [1]. State-of-the-art MOSFET devices suffer more and more with impurities diffusion during thermal processes due to their extremely sharp doping gradient, usually going from 10^{20} atoms/cm^3 p-type dopants to 10^{20} atoms/cm^3 n-type dopants in just a few nanometers. In comparison, JL-FET devices have the same doping concentration throughout the entire device, thus its diminished dopant diffusion rates. Besides the reduced fabrication costs that stems from the possibility of using standard thermal annealing and fewer ionic implantation steps, the JL-FET also stands out due to its performance. The electrical current density is distributed through the thickness of the substrate[1], the charge carriers involved in the current are of the majority type[1], and some of the charge scattering phenomena can be mitigated by polarizing the gate in a flat-band condition[1], this allows a greater current for a given device's dimensions.

This work aims to demonstrate that the anisotropic silicon etching in NH_4OH solution, which is known to etch silicon [5], has viability in fabricating the channel of JL-FET devices, as opposed to techniques more frequently used in the literature such as electron lithography [1] and focused ion beam milling [2]. Other works also used a tetramethylammonium hydroxide (TMAH) solution to fabricate devices with gate lengths close to 3nm [3, 4]. The TMAH solution is based on the NH_4OH solution.

3. Experimental methods

JL-FET devices fabrication on a Silicon-On-Insulator (SOI) substrate was simulated in Silvaco's Athena. This environment simulates the fabrication process and allows to plan thermal processes, ionic implantation and more. These models were loaded onto Silvaco's Atlas in order to simulate the devices' electrical characteristics. The end goal of channel thickness was set and the devices functionality was confirmed. The subsequent device fabrication was planned using information from the simulation.

The device fabrication was carried out on 340nm Si over 400nm SiO_2 SOI wafers that were cleaned using standard RCA cleaning. Wet oxidation and silicon oxide etching in a HF buffer solution was used to thin the substrate to approximately 200nm. The wafers were then subjected to ionic implantation of phosphorus at 50keV, with a dose of 10^{13} atoms/cm^2 and the dopant activation was carried out in a 1000° C conventional oven in inert gas for 30 minutes. The active region was defined through lithography, sputtered aluminum deposition, lift-off and ICP-RIE silicon etching. A silicon oxide hard mask was then grown through ECR plasma, defined by lithography and etched in HF buffer solution. The anisotropic silicon etching in NH_4OH solution then took place for 40 seconds. SEM imaging was used to confirm the wet etching process. The gate oxide was silicon oxynitride grown through O_2/N_2 ECR plasma. The gate metal was defined by lithography and lift-off, and was made out of sputtered TiN. The oxide covering the drain and source regions was etched using lithography and HF solution etching, and the metallic pads were deposited by sputtering. Final annealing was carried out in 5 minutes steps, on a conventional oven at 450° C in forming gas (H_2).

After each annealing step, the devices' I-V curves were measured on a Keithley probestation. With the annealing and electrical measurements done, cross-sections images were extracted using Ga^+ Focused Ion Beam milling and SEM imaging.

4. Results and discussion

Fig. 1 shows clearly the expected geometrical structure. Measurements made using an image editing software showed that the thickness of the channel after NH_4OH solution wet etching was approximately 65nm and the channel walls had the characteristic angle between the (100) and (111) crystallographic planes, approximately 57 degrees. The rounded edges are the result of meta-stable (311) planes that occur during anisotropic etching [6]. These results show that it is

indeed possible to thin the channel's thickness in a satisfactory manner using silicon wet etching in NH_4OH solution.

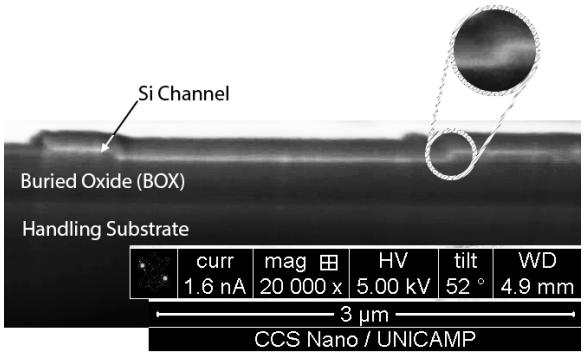

Fig. 1. Cross-section SEM image of the fabricated device.

The electrical measurements carried out after each annealing step yielded varying degrees of success, and the measurements that showed the best contact quality and transistor behavior were those made after 20 minutes of annealing. As expected, most of the measurements showed diminished effect of the gate voltage on the current, this happens because at 65nm channel thickness the depletion region induced by the gate isn't wide enough to deplete every charge carrier, the device's threshold voltage becomes very negative, and the device act as a gated resistor for most of the V_{DS} range. As Fig. 2 illustrates, the electrical contacts presented low quality and acted like Schottky diodes, distorting the I-V measurements, this happens because the final doping concentration was not high enough on the source and drain regions to maintain ohmic contacts.

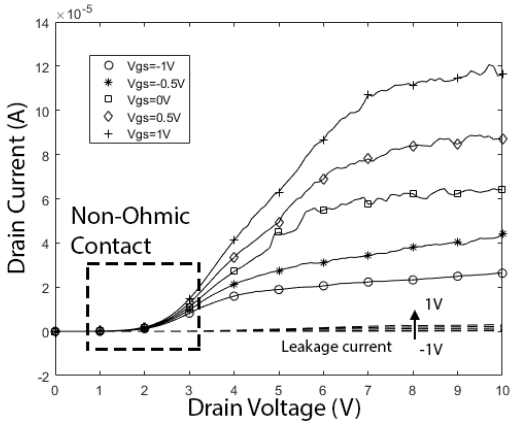

Fig. 2. I_D xV_{GS} curves of the fabricated device, dashed lines represent the gate leakage current I_G.

Despite the device's inability to act as a switch due to its negative threshold voltage, the I_D x V_{DS} results indicate the occurrence of transistor behavior and low gate leakage current.

5. Summary and conclusion

The fabricated device presented transistor behavior with well-defined triode and saturation regions, but could not achieve cut-off. Further tuning of the NH_4OH wet etching process can lead to JL-FET devices that rival the electrical performance of state-of-the-art enhancement-type MOSFET devices.

Therefore, this work demonstrated that the anisotropic silicon etching in NH_4OH solution is a viable technique to thin a silicon-based JL-FET device's channel substrate.

Acknowledgments

The authors would like to thank CCSnano staff for the support during device simulation, fabrication and characterization. This work is supported by INCT-Namitec, SisNANO, CNPq, Fapesp and CAPES.

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Extended Application of BSIM3v3 Model through Code Development

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1. Abstract

The aim of this work is to present the results of a created code based on the BSIM3v3.1 model for MOSFET transistors. This code was made through the implementation of the characteristic equations of the BSIM3v3.1 model in MATLAB environment, aiming at the versatility of the model simulation, which allows a more complete and deep study of its characteristics and parameters.

In this study, the focus will be on the nMOSFET, but implementation of the code was performed for both nMOSFET and pMOSFET types.

2. Introduction

MOSFETs have become by far the most widely used electronic device, especially in the design of integrated circuits (ICs) [1]. A MOSFET is composed of a channel of semiconductor material of N or P type, named nMOS or pMOS.

BSIM3v3.1 is one of the latest physics-based, deep-submicron MOSFET models for digital and analog circuit designs from the Device Group at the University of California at Berkeley. BSIM3v3.1 has been extensively modified from its previous release (BSIM3 Version 2.0) [2].

Usually, this model is implemented in SPICE simulators, allowing its application to circuit simulation, with very realistic results. SPICE simulators are, nowadays, very user friendly, fast and accurate. On the other hand, such simulators restrict the model use, by limiting variable and parameters input and observation. This work shows how a code-level model implementation can be useful for a deeper device and model analysis.

3. Model Characteristics

A complete set of curves $I_D(V_{DS})$ for de nMOSFET, called "output characteristics" is shown in Fig.1.

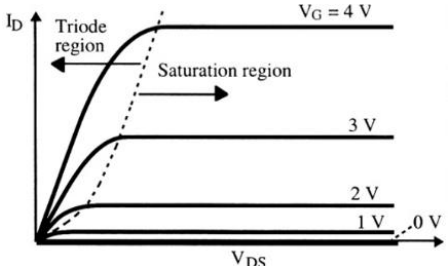

Fig. 1 - $I_{DS}(V_{DS})$ characteristics for VG=0,1,2,3,4V and VTH0=0,7V [4].

Fig. 2 shows the $I_D(V_{GS})$ characteristic of an nMOS transistor operating in saturation.

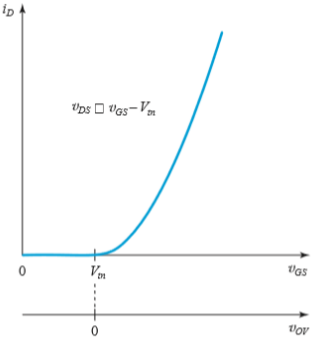

Fig. 2 - The $I_{DS}(V_{GS})$ characteristic of an nMOS transistor operating in the saturation region [1].

The BSIM3v3.1 model has evolved through three different versions. The third version is the one used for the code development. It has become an industry standard for modeling deep-submicron MOS technologies and includes the first and second's characteristics: original basis for the model, corrections of mathematical error and introduction of new parameters. This allows users to accurately model the MOSFET over a wide range of channel lengths, channel widths for present and future technologies. The model is suitable for both digital and analog applications due to better modeling of its output conductance [3].

Moreover, BSIM3v3.1 still relies on a formulation to model various short-channel and high field effects such as threshold voltage roll-off, mobility reduction due to vertical field, carrier velocity saturation, channel-length modulation, etc. [3].

The model had its 39 main equations used for the code implementation. The main equation of the model is described below:

$$I_{ds}(i) = \left(\frac{I_{ds0}}{1+\left(\frac{rds*I_{ds0}}{vdseff}\right)}\right) * \left(1 + \left(\frac{vds-vdseff}{va}\right)\right) * \left(1 + \left((vds - vdseff) * \left(\frac{1}{vascbe}\right)\right)\right) \quad (1)$$

Where:

I_{ds}=drain-to-source current; *rds*=drain-source on resistance; $I_{ds}0$=initial I_{ds}; *vdseff*=effective drain-source voltage; *vds*=drain-source voltage; *va*= early voltage; and *vascabe*=early voltage due to substrate current induced body effect.

4. Discussion and Results

With the use of simulation software it is possible to predict the operation of almost every existent circuit. Using SPICE as an example, the user can simulate its circuit of interest with discrete components and circuits implemented in Integrated Circuits. With this tool, it is possible for a circuit to be simulated before its layout is implemented, since the designer will only begin designing after the circuit analyzes.

However, such simulation software, again taking SPICE as one of the possible examples, does not allow the complete analysis of all parameters of the circuit individually, since they focus on the analysis of the output components of the simulation.

As a solution, a code that allows the analysis of all the parameters that involve the equation transistors based in BSIM3v3.1 Model was designed. Fig. 3 and Fig. 4 represent the characteristic curves of a nMOSFET generated by the code created in MATLAB, which are the $I_{DS}(V_{DS})$ and $I_{DS}(V_{GS})$ curves. The whole code has its equations based in the "Eldo Device Equations Manual" [5].

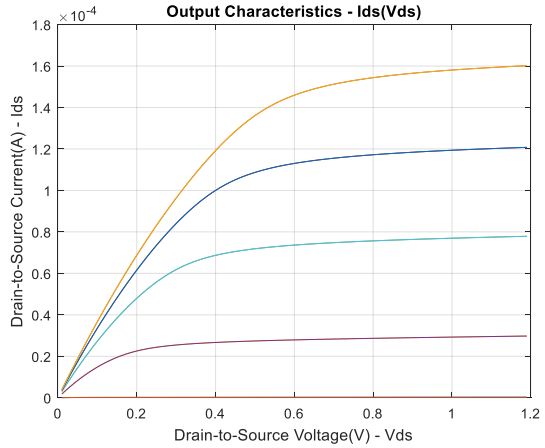

Fig. 3 – $I_{DS}(V_{DS})$ Graphic generated by the implemented code in MATLAB

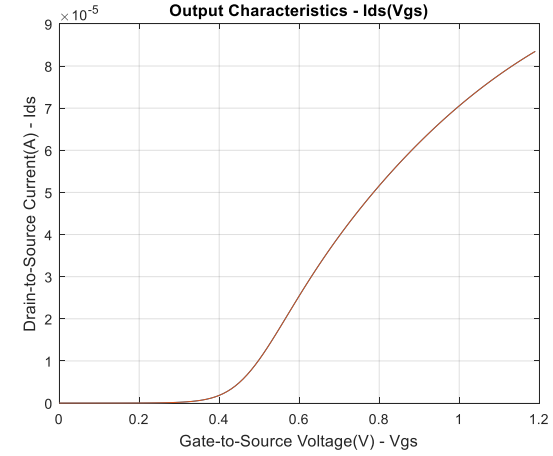

Fig. 4 – $I_{DS}(V_{GS})$ Graphic generated by the implemented code in MATLAB

Comparing Fig. 1 and Fig. 2 to with the reference curves presented, the code made in MATLAB has correctly reproduced the nMOSFET characteristic curves for the BSIM3v3.1 model and it can now generate several graphs with any parameters for the study of the influence of the variables on the transistor. For instance, Fig. 5 shows the characteristic curve of the effective mobility for a gate-to-source voltage variation.

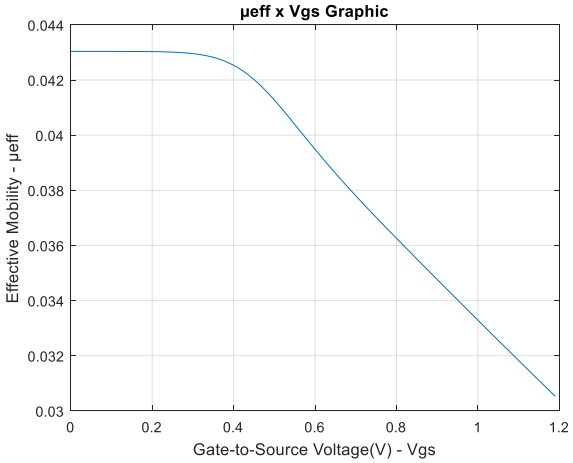

Fig. 5 - Effective Mobility vrs. Gate-to-Source Voltage generated by MATLAB

In order to allow that the code work with any technology, an auxiliary file was created only with the values used by the variables of the current model, which can be replaced according with the required technology.

5. Conclusion

The aim of this work was the creation of a code in the MATLAB software to obtain a fast and versatile simulation response allowing the analysis of all the parameters that involve the equation transistors based in BSIM3v3.1. As the code could correctly reproduce the main curves of the nMOSFET, it can reproduce any parameters characteristics, streamlining further study of the influence of variables in transistors. The authors intend to publish the code in a user-friendly interface, as soon as it has been fully tested for some different technologies.

Acknowledgments

The authors would like to thank the financial support provided by CAPES and CNPq.

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Improved Controller for a Large Area Tactile Sensor based on Fabric

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1.Abstract

This paper has as main objective to describe the controller for a sensitive fabric, used to implement a touch sensor. The controller is based on the connection between an FPGA and a fabric with an intrinsic RC (resistor-capacitor) network. The sensor was developed to be a wearable device for people with tactile disability. The reference designs were revised and the circuits were time-optimized and reallocated to a faster FPGA, in order to improve stability and reliability of the sensor. The resulting assembly showed the aimed stability.

2.Introduction

Wearable devices have been developed recently and some of them are already commercially available. The main challenge for large area touch sensing devices is their compatibility with user skin needs, specially its comfort characteristics. The inclusion of conductive wires and electronic components has to be minimum, in order to maintain the fabric comfort. Consequently, the interface circuits have to deal with fragile and noisy signals. FPGA is a flexible and programmable semiconductor integrated circuit, it is based on a large array of configurable logic blocks contained in the same integrated circuit [1]. The main advantage is its flexibility and speed.

***Fig. 1** – DE2-70 of Altera.*

Responsible for processing digital information, the FPGA is used with the auxiliary computational tools, Quartus II and the circuits were described in VHDL, a hardware description language [2].

Some conductive fibers were inserted into the fabric structure, as part of the fabrication process. These fibers are connected to discrete passive components, and then to FPGA pins directly. A pin is used to stimulate the network, through a change in the logic level, and the other "reads" the fabric response delay. The following equations are necessary to understand the behavior of the simplest resistor-capacitor network, where E is the stimulus' amplitude applied to the circuit.

Capacitor's voltage:

$$Vc(t) = E - E * e^{-\frac{t}{R*C}} \qquad [3]$$

Resistor's voltage:

$$Vr(t) = E * e^{-\frac{t}{R*C}} \qquad [3]$$

Current through time:

$$i(t) = \frac{E}{R} * e^{-\frac{t}{R*C}} \qquad [4]$$

Based on the equations, the higher the resistance and capacitance, higher is the time so that the capacitor gets full charged or completely discharged, following the temporal relationship:

$$t=R*C \qquad [4]$$

Furthermore, it's important to highlight the fact that the touch of our fingers in a close distance to a capacitor causes a rise on the total capacitance of the circuit. It happens because the finger capacitance is created by the minerals present in our bodies, and as the body has a much larger area than the sensor, it works as earth to the capacitor from the finger.

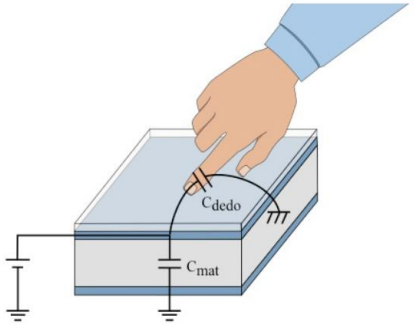

***Fig. 2** – Finger capacitance interference on the circuit [3].*

These concepts and the article: ‘’A New Textile Tactil wide-area Sensor for Clothing’’[5] were essential references to elaborate the touch tissue, which is based on the emission of pulses to a RC circuit and the detection of the response’s delay by the FPGA.

3.Delay evaluation

The delay is measured and quantified into an integer number using as reference the internal clock from the FPGA. A digital low-pass circuit is implemented, in order to reduce high-frequency noise. After that, the numerical value obtained for each circuit is sent from a Bluetooth module to an Android smartphone, by using the Bluetooth Electronics app as an interpreter to the module’s signal.

Simplifying the device’s function, the delay from all the circuits are equal without the tough, while recognizing that they are under the same conditions. However, when there is the finger’s presence, the delay of response on each circuit changes based on the proximity of the touch to the circuit. The weighted average of the measured delay from each circuit by the FPGA is responsible for providing the coordinates from the touch.

Fig. 3 – *Touch tissue developed by the Department of Electrical Engineering from Centro Universitário FEI.*

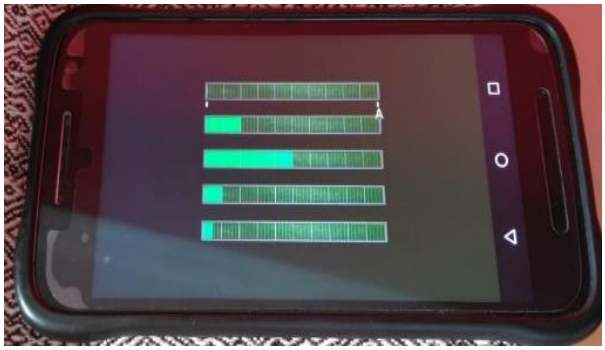

Fig. 4 – *Capacitor response delay in each circuit, represented on Bluetooth Eletronics App.*

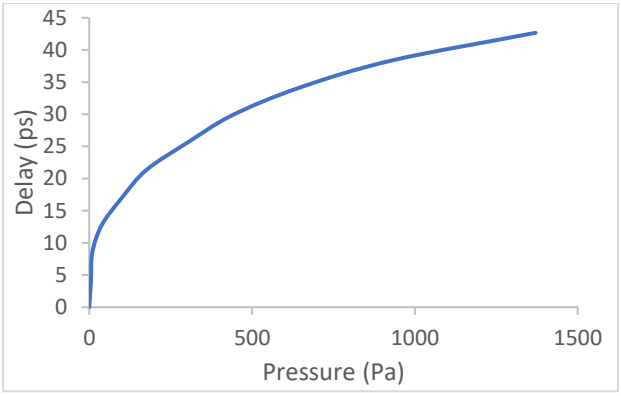

Fig.5 – *Delay in one RC circuit, in function of pressure*

4.Conclusion

The touch device based on RC circuit and FPGA presented in this paper has shown itself as promising, since the circuit’s response to the signal interpreter is almost instantaneous. Furthermore, it’s important to stablish a referential value to the delay, based on the environmental conditions. By doing so, the data sent to the interpreter will be determined only by the finger influence, excluding the natural delay response from the RC circuit.

Acknowledgments

The authors gladly thank CAPES and CNPq for the financial support.

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Transient Measurements of Self-Heating Current Degradation in Junctionless Nanowire MOSFETs

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1. Abstract

This paper examines the experimental results on the occurrence of self-heating effects in junctionless nanowire transistors fabricated in SOI technology using the Pulsed IV method. Results are analyzed through current transients and self-heating is verified in the drain current degradation.

2. Introduction

Self-heating is a phenomenon inherent to the physics of semiconductors and it is related to the transistor's thermal profile. It consists in temperature rise due to power dissipation in form of heat energy during device operation, caused by current flow in the transistor's channel [1]. The thermal conductance held by silicon dioxide is about 100 times lower than the silicon's thermal conductance, which results in lower heat dissipation from the device. This makes the SOI technology highly susceptible to self-heating, due to the presence of a thick buried oxide layer under the active silicon region [2]. It is also known that thermal confinement also contributes to the occurrence of self-heating, which makes SOI nanowires more difficult to dissipate heat because of the smaller area and insulator confinement.

Within the effects caused by self-heating, current degradation is one of the most commonly observed, being a consequence of carrier mobility degradation caused by a rise in scattering phenomena that have dependence with temperature. The current degradation can be verified not only in permanent regime, where the drain current in I_D-V_D curves are reduced, leading to negative output conductance in extreme cases [3], but also in transient regime, where the effects caused by temperature rise are observed through current transients, when fast pulsed measurements are used.

This technique is known as the Pulsed IV method and, although it allows the verification of the drain current degradation as it is happening, this is only achievable by creating pulses with very fast rise times [4], which is not always possible considering the equipment's limitations. The main problem that limits the success of the pulsed measurement is related to curve distortion caused by current overshoot, which is the rise in the current response to a fast voltage impulse above the expected current value, where damped oscillation is observed until settling is achieved. Like the intensity of self-heating effects, the occurrence of overshoot is highly dependent on the device being measured and its architectural characteristics.

In this work, an analysis on the transient performance of junctionless nanowire MOSFETs fabricated in SOI substrates is presented through experimental pulsed measurements, with focus on the verification of self-heating effects in the drain current by using the Pulsed IV method.

3. Device Characteristics

The measured JNTs were fabricated in a 145 nm thick SOI wafer, having a HfSiON and SiO_2 gate stack, with an EOT of 1,3 nm, fin height of 10 nm, fin width from 30 to 240 nm and channel length from 20 to 400 nm. Both single fin and 10 fin transistors were measured. The doping profile was previously estimated in $7.7.10^{18}$ cm^{-3}. Figure 1 presents a schematic view and the longitudinal section of the junctionless nanowire.

4. Results and Analysis

For all the measured transistors, the first step taken was to obtain the I_D-V_G curves to extract the threshold voltage of each device, which allowed gate biasing using the gate voltage overdrive (V_{GT}). The first devices to be measured through Pulsed IV were the multifin transistors, with varying fin width for a 40 nm channel length. Figure 2 shows the current transients for these measurements.

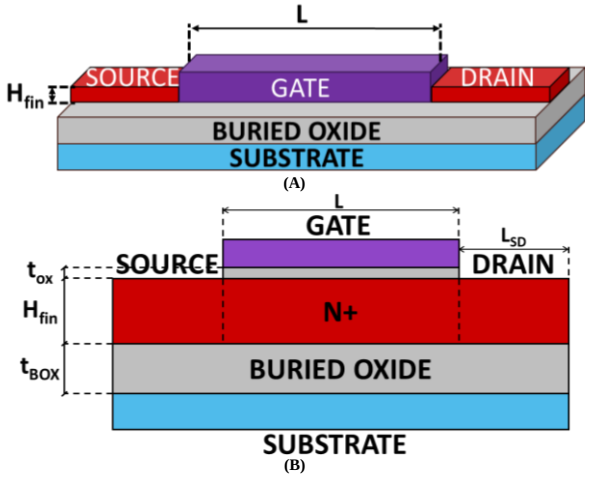

Fig.1. *Three-dimensional scheme (A) and longitudinal section (B) of a junctionless nanowire transistor.*

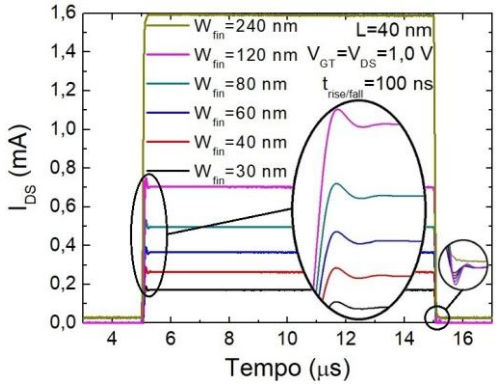

Fig.2. *Current transient response to pulsing the gate of multifin junctionless nanowire transistors.*

The set of multifin transistors presented the most distortion due to overshoot, even if the rise time is slowed down, which can be confirmed by the repetition of the distortion in the fall time region. The only case where no overshoot is seen is for the 240 nm W_{fin} transistor, and yet no current degradation due to self-heating is observed, since the multifin current values are high, but the drain current flown in the individual fins is 10 times lower than the one shown in the curve.

Therefore, a set of single fin transistors with fin width of 240 nm was measured for different channel lengths, varying the pulse's rise time. The result for the 500 ns rise time is presented in Figure 3, where no overshoot is seen, and current degradation is noticed after the pulse rise. When a faster t_{rise} is used, the current peak is increased, since the sooner the current is

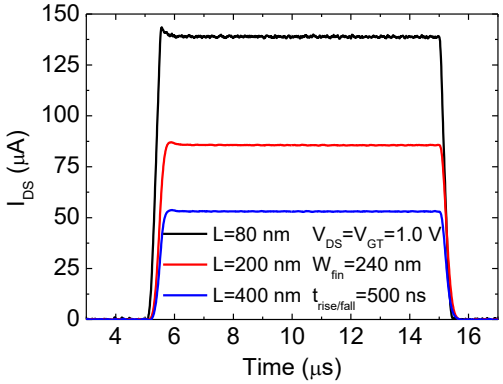

Fig.3. *Current transient response to pulsing the gate of single fin junctionless nanowire transistors with W_{fin} of 240 nm.*

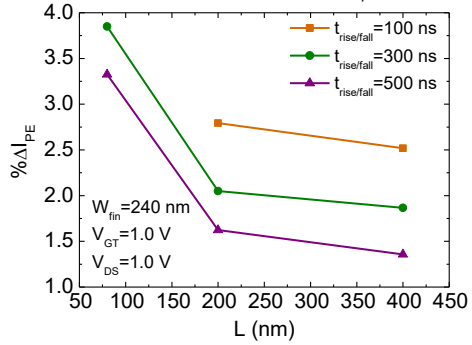

Fig.4. *Current degradation percentage as a function of channel length for different rise and fall times.*

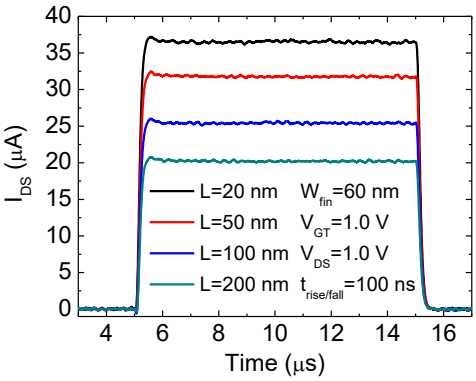

Fig.5. *Current transient response to pulsing the gate of single fin junctionless nanowire transistors with W_{fin} of 60 nm.*

acquired, the less heated up the device is. Also, a biggest current degradation can be seen for the shortest transistor. To make a fair comparison, it was calculated the percentage of current degradation from peak to the degraded part ($\%\Delta I_{PE}$) and presented as a function of channel length in Figure 4. By reducing the channel length a stronger current degradation is observed since a higher current generates more heat. The highest degradation percentage was calculated at 3.85%.

Finally, in Figure 5 a similar set of transistors, but with fin width of 60 nm, was tested. Since these narrower transistors have lower current levels, the degradation due to self-heating is less visible. This is confirmed when calculating the current degradation percentage, where a slightly lower $\%\Delta I_{PE}$ is obtained.

5. Conclusions

This paper analyzed the transient response of SOI junctionless nanowire transistors to the Pulsed IV method. Experimental results showed that even for high gate overdrive, the effects provoked by self-heating in the drain current didn't result in relevant current degradation in these devices, being lower than 4%.

Acknowledgments

The authors acknowledge CAPES for the financial support.

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Study of Photoconductive Switches for Reconfigurable Antenna Application

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1. Abstract

This study presents an optically reconfigurable antenna design for wireless applications and investigates three possible photoconductive switches for application. Simulation and experimental tests demonstrate that the antenna operates at 5.8 GHz when the switch is not illuminated, changing to 2.0 GHz when exposed to a laser light. A horizontal and vertical photoresistor and a PIN diode acting as optical switches are simulated and compared. It is shown that the vertical photoresistor has the largest off to on resistance at the 5 GHz frequency range, thus being the best choice as a switch.

2. Introduction

The use of telecommunication systems has grown rapidly in recent years. With increase in demand, adaption of the antenna technology is exploited to meet new market requirements [1]. Reconfigurable antennas have received great attention in recent years due to their flexibility to operate at multiband frequencies, an important feature for new wireless technologies [2]. They are manufactured so that some of their parameters, such as the operation frequency, for example, can be changed on the fly to suit the requirements of the system.

The reconfigurable technique can be implemented using PIN diode, varactor, RF MEMS, or photoconductive elements [4]. In this work, a semiconductor photoconductive device has been used, since 1) it does not require a bias line, which eliminates a possible interference of the DC bias, and 2) it facilitates the integration of the antenna in a photonic circuit. However, the most important reason for this choice is that the photoconductive switches have fast switching speeds in the order of nanoseconds, being superior in terms of performance when compared to RF MEMS, PIN diode [4].

In this work, a reconfigurable E-shaped antenna is designed to work at 2.0 GHz and 5.8 GHz. Experimental tests have been performed to validate the reconfigurable antenna design. Three possible implementation of photoconductive switches are investigated and simulated: a horizontal photoresistor, a vertical photoresistor, and a PIN diode.

3. E-Shaped Antenna Design and Measurement

A microstrip antenna consists in a small sheet of metallic material printed on a substrate of dielectric material. Here, FR4 with dielectric constant of 4.4 is used as substrate, the metal strip is made of Cu. The ground is a second strip at the bottom of the antenna. The structure of the E-Shaped antenna is shown in Figure 1 together with its dimensions.

The designed antenna has been simulated using HFSS ANSYS. A layer, whose resistivity can be varied, implements the switch effect. Thus, the switch resistance variation from off to on states can be taken into account. Figure 2(a) shows the simulated return loss of the antenna as a function of frequency considering the off and on states, represented by a resistance of 6 kΩ and 130 Ω, respectively. In the off state, the central arm of the antenna of Figure 1 is not fed and a return loss of -22 dB at 5.8 GHz is obtained, while for the other frequencies it is above -10 dB. Under this condition, the operation frequency of antenna is then 5.8 GHz. In the on state, all arms of the antenna of Figure 1 are fed, the return loss at 5.8 GHz increases above -10 dB while at 2.0 GHz decreases to -22 dB. This shows the operation frequency switch from 5.8 GHz to 2.0 GHz.

Figure 2(b) shows the experimental measurement of the return loss. The used photoconductive switch is the commercial LDR (Light Dependent Resistor) GL5528, where 9 kΩ and 130 Ω are the measured resistances for the off and on state, respectively. In off state, a return loss of -17 dB is obtained at 5.8 GHz and of -7.9 dB at 2.0 GHz. In the on state, when a laser light activated the LDR, the return loss reduced to -23.9 dB at 2.0 GHz.

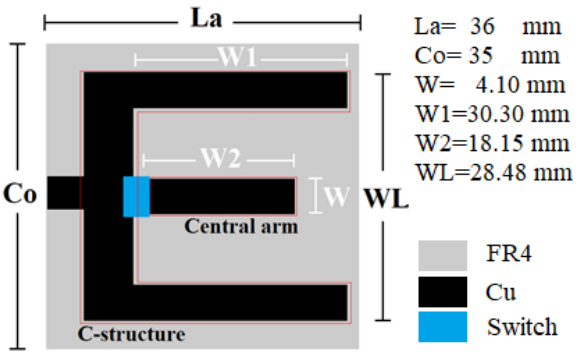
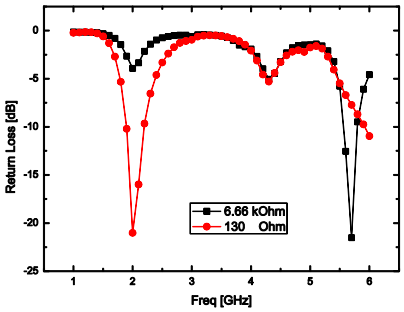
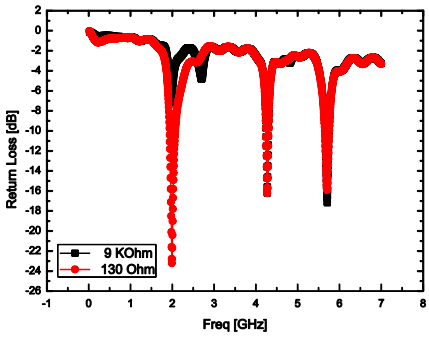


Figure 1: E-Shaped geometry and dimensions.



(a)



(b)

Figure 2: Return loss of the antenna for the off (black line) and on (red line) states. (a) HFSS simulation. (b) Experimental measurement.

4. Photoconductive Device Design and Simulation

Three semiconductor devices, a horizontal and vertical photoresistor and a PIN diode, have been investigated as the photoconductive switch for the antenna. These devices have been simulated using Athena and Atlas from SILVACO. The photoresistors are made of p-type Si substrate with a concentration of 10^{13} cm^{-3}. Their absorption area is 1.0 x 2.0 mm^2 and the substrate is 300 μm thick. The horizontal device has both Al electrodes deposited on top of the wafer, while the vertical device has an electrode at the bottom of the substrate. The PIN diode is made on a p-type substrate with a concentration of 10^{15} cm^{-3}. The N region is created by an ion implantation of phosphorus with a dose 10^{15} cm^{-2} and energy of 30 keV.

The devices are simulated in the off and on states. In the off state, the devices do not receive the laser light, so their conductivity is at minimum value. In the on state, the device is activated, i.e., the device is exposed to laser light, a photogeneration process occurs, which increases the charge carrier concentration and, consequently, the device conductivity. The devices are illuminated by a light with a wavelength of 532 ± 10 nm and a power of 98 mW. The resistances have been extracted from a DC and also from an AC analysis at 5.0 GHz. The results are shown in the Table I.

Table I: Simulated resistances in off and on states.

Switch	Horizontal		Vertical		PIN diode	
State	Off	On	Off	On	Off	On
R_{DC} (kΩ)	25.6	0.92	15	1.5	6400	0.028
R_{AC} (kΩ)	25.5	0.83	13.2	0.26	0.025	0.021
R_{off}/R_{on} (DC/AC)	27.9	30.7	10	51.8	2.1 M	1.2

From Table I we can see that the DC ratio between R_{off} and R_{on} for the PIN diode is 2.1 x 10^6, being much larger than for all other devices. Thus, the PIN diode seems to be the better choice as a switch (off state has a very high resistance and on state has a very small resistance). The horizontal photoresistor shows the second better performance followed by the vertical photoresistor. However, considering the AC analysis at 5 GHZ, a different result is obtained. Here, the PIN diode shows a small resistance for both, the on and the off state, due to the admittance of junction [5], yielding a ratio of only 1.2. Therefore, it does not work as a good switch. For the AC analysis, the vertical photoresistor shows the largest ratio, 51.8, between the off and the on states, followed by the horizontal photoresistor with a ratio of 30.7. Thus, the vertical photoresistor functions as a better optical switch in the range of frequencies that the reconfigurable antenna works.

5. Conclusions

A reconfigurable antenna that switches its operation frequency from 5.8 GHz to 2.0 GHz was designed, simulated and experimentally validated. At 5.8 GHz a reflection coefficient of -17 dB was measured. After the switch was illuminated, the reflection coefficient at 2.0 GHz reduced to -23.9 dB, showing that the antenna can now operate at this frequency. The electric behavior of three different switches was simulated and compared. It has been shown that the vertical photoresistor works as a better switch in the range of 5 GHz. The PIN diode, despite having a great difference between the resistance at the off and on states in DC, shows a resistance of tens of ohms only at high frequencies, so it cannot work as a suitable switch for the proposed antenna.

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Foundry Polymer-Based Photonic Devices

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1. Abstract

This manuscript presents preliminary results of the development of photonic devices based on high-volume CMOS foundry process for polymer inverted-rib waveguides. The CEITEC S.A. facilities were used to fabricate the 150 mm wafers. Photomask design and manufacturing, as well as wafer post-processing were carried out at CTI. A summary of the device processing and characterization, as well some preliminary optical results are presented. Spectral filters with free spectral range (FSR) of about 1 nm are demonstrated.

2. Introduction

Polymer based photonic devices [1], [2] are of interest due to their potential use of high-volume manufacturing techniques. Moreover, the increasing availability of efficient functional materials has lead to desirable functions, such as electro-optic effect, photo-detection and photo-emission. Often these are added through "doping" of a host polymer with chromophores, dyes, quantum-dots, to name a few additives. Thus integrated photonic devices with applications in communications and sensing can be produced in short cycle and at low cost.

In this paper we present the first foundry fabrication of photonic integrated circuits in Brazil. We focus on the design, manufacturing and characterization of ring resonator notch filters.

Fig. 1 shows a schematic of the platform used to define the guiding structures. The inverted-rib waveguide structure [3] was used, as it enables direct use of the microelectronic capabilities of CEITEC´s foundry facilities. For the polymer guiding layer we used spin-coated SU-8 polymer due to its adequate index of refraction, and for future comparison with other fabrication techniques.

Fig.1. *Schematic of the inverted-rib waveguide.*

The layout of integrated photonic components (splitters, combiners, directional couplers, ring resonators, among others) is shown in Fig. 2. This layout was transferred to a photomask by means of a Heidelberg DWL 66FS system. This transfer is done at 5x the size to account for the latter 5x reduction during stepper photolithography. The 20 mm square die was stepped in an array of 7x7 rows and columns.

Details on mask manufacturing using repurposed mask blanks will be published elsewhere.

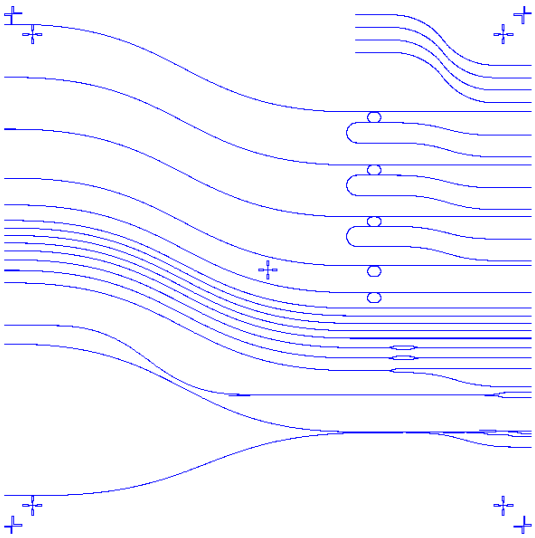

Fig.2. *Layout.*

3. Fabrication and Results

A. Sample Preparation

The wafer processing starts with deposition of a thick SiO_2 layer onto a Si substrate. This SiO_2 layer is deposited by using plasma chemical vapor deposition (PECVD) and has 4 µm of thickness. After the optical lithography step, the layout mask is transferred to the SiO_2 layer by dry etching using reactive ion etching (RIE).

Fig. 3 shows a scanning electron microscopy (SEM) image, in tilted view, of a test sample in the region of the directional coupler that composes the ring resonator structure. One can notice that high quality waveguide channels and short gap regions can be obtained. In this example, waveguide channels are about 2.2 µm wide and 570 nm deep. Also, the gap between them is as low as 400 nm wide.

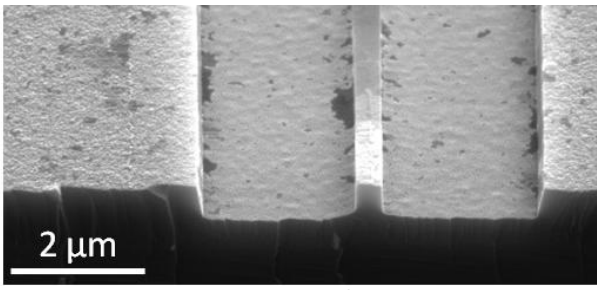

Fig.3. *Cross-sectional tilted view from a direction coupler before resist deposition by spin coating.*

The wafer was diced to expose the waveguide facets and finally a SU-8 (photoresist) layer of about 780 nm thick was deposited by spin coating in order to define the guiding region of the inverted-rib waveguide based devices. The viscosity of SU-8 2100 (75% solid) was reduced by diluting it to 14% solid with cyclopentanone so that the desired thickness could be obtained by spin coating. The refractive index of SU-8 is about 1.57 and the SiO_2 is about 1.48.

B. Optical characterization

Optical characterizations were carried out by the edge-coupling approach (with lensed fibers) using a Keysigth 81636B Fast Power Sensor Module and a 81980A Tunable Laser C band with electric field polarized parallel to the substrate (quasi-TE mode). The equipment is computer controlled and the data acquired using Keysigth Photonic Application Suite. Fig. 4 shows one photonic chip mounted on the optical setup for characterization.

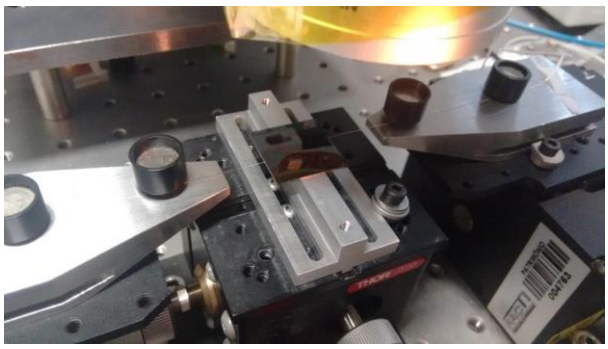

Fig.4. *Photonic chip mounted on the optical setup for characterization.*

Fig. 5 shows the transmission power (excluding coupling and propagation losses) as a function of wavelength for one of the fabricated filters based on ring resonators.

These results shows the response of a high resolution filter, measured around the C-band, with FSR = 1 nm and extinction rate of about 5.5 dB. We believe after performing some geometric optimization and by improving the quality of the waveguide facets (by polishing), those filters can be promising for applications in communications or sensing at low cost.

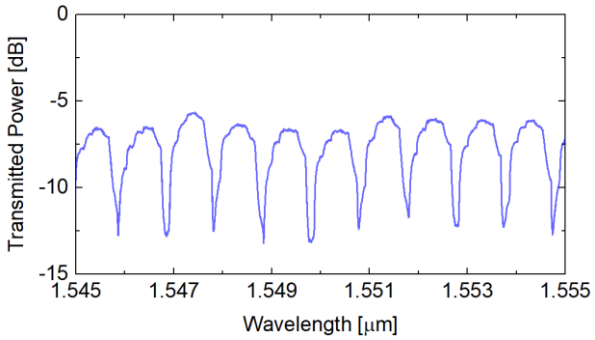

Fig.5. *Power transmission spectrum.*

4. Conclusions

We have demonstrated initial transmission results of polymer photonic devices manufactured at CEITEC for the future development of high-volume photonics devices based on CMOS foundry process. High-resolution spectral filters based on inverted-rib waveguides having polymer (SU-8) as guiding layer were fabricated and optically characterized. Although, the optimization of the process and devices are at the initial stage, we believe these preliminary results may be promising for applications in communications or sensing at low cost.

Acknowledgments

The authors would like to thank the technical staff of COLAB at *Centro de Tecnologia da Informação (CTI) Renato Archer* for photomask manufacturing, dicing, and polishing. Funding was provided by the *Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq)*, #456294/2013-9 and #300594/2017-8, for the financial support. We acknowledge use of CTI´s Heidelberg DWL66FS FAPESP multiuser equipment EMU 09/54045 for mask production.

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Ultra-Thin Buried Oxide SOI MOSFET Device Analyses

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1. Abstract

In this paper, the Fully Depleted Ultra-Thin Box Silicon On Insulator (FD UTBOX SOI) device will be investigated through numerical simulations at different bias conditions. The simulation results showed that the FD SOI UTBOX device can be operated as a quasi-PD device by changing back gate bias (Vsubs).

2. Introduction

SOI technology has emerged as an alternative improvement of CMOS (Complementary Metal Oxide Semiconductor), and its manufacture is used a thin layer of silicon oxide which is isolated from the device substrate, as shown in Fig. 1[1].

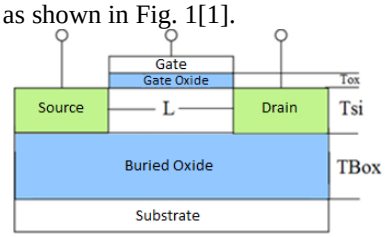


Fig.1. *UTBOX SOI nMOSFET indicating Source, Drain, and different parameters like Tox, Tsi, TBox and the channel length (L).*

The combination of a Fully-Depleted Thin-film with an Ultra-Thin Buried Oxide further enhances the control over the short channel effects (SCEs), so that UTBOX devices are promising candidates for sub-22 nm technology nodes [2]. Moreover, these devices are also promising for further downscaling of memory cells with one transistor and no capacitor 1T DRAM [3]. The presence of the memory effect (floating body), which relies on holes injection into the device substrate can be assessed by the device latchup/hysteresis measurements.

The conventional latchup definition states that this phenomenon is an extreme case of the floating body effects and occurring at a sufficiently large drain to source bias [1]. The latchup effect is usually reported in partially depleted (PD) SOI, although it is also shown in FD SOI with or without UTBOX [4].

Another advantage of UTBOX SOI is that its threshold voltage (VT) can be modulated without changing the doping concentration of the film. Due to the very thin BOX, the VT is also modulated when the back channel changes from inversion to depletion or accumulation. Then, VT is controlled by the body factor [5].

3. Methodology and Results

The n-channel device analyzed, have been fabricated on SOI substrates with a 20 nm buried oxide (TBox) and Si film of (Tsi) 20 nm. The channel is undoped, L = 170 nm and the gate dielectric (Tox) consists of 2.5 nm SiON. More process details can be found in "Reference [6]."

Fig. 2 shows the experimental and the simulated curve of drain current (Id) versus gate voltage (Vg) in the saturation region with drain voltage (Vd) of 1.5 V. Simulations were adjusted from experimental results of electrical characterizations carried out at the interuniversity microelectronics center (Imec) of the Catholic University of Leuven in Belgium. A good correlation between experimental and simulated data is observed. The 3-D numerical simulator used is Atlas of Silvaco [7].

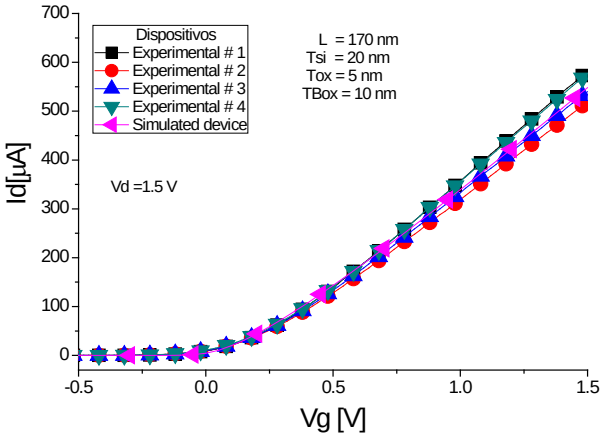


Fig2. *Experimental and simulated curve of drain current (Id) versus gate voltage (Vg)[8].*

Fig. 3 shows the simulation results of drain curves on saturation operating for different conditions of front gate (Vg) and back gate biases (Vsubs). It can be seen that the threshold voltage is reduced when the back gate bias (Vsubs) is increased.

When Vsubs increases, it is observed that the current conduction occurs across in the volume of the silicon film (fig.4b and fig.5.b) i.e. in this case the inversion occurs in the entire channel. In this biasing condition, the device operates as a fully depleted.

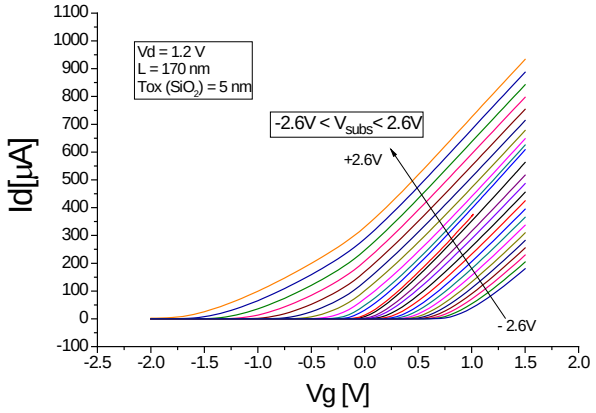
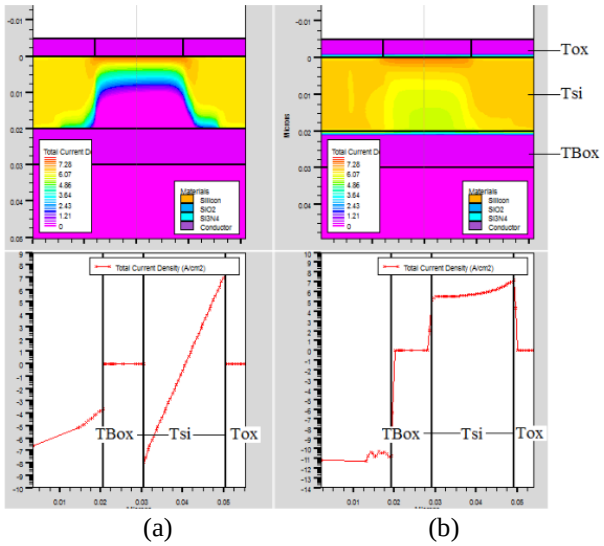
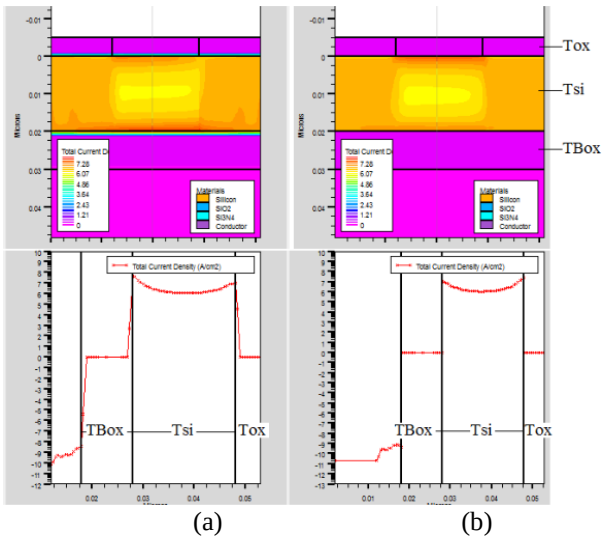


Fig3. *Drain Current (Id) as function of the front gate bias (Vg) with Vd = 1.2 V and the back gate bias (Vsubs) is changed from -2.6 V to 2.6 V[8].*



(a) (b)

Fig.4. *Overall current density with subs = -2.6V; Subs = 0.0V. The vertical section illustrates that the current is concentrated in the upper part of the channel as seen by the increased straight in TSi [8].*



(a) (b)

Fig.5. *Overall current density with Subs = 5V; Subs = 1.0V[8].*

However, when a large positive back gate bias is applied (Fig.5a), the back interface is inverted so that the conduction in the device begins and be greater at the bottom of the channel than at the top (the reverse occurs at the bottom of the channel as show in Fig. 4a) analyzed. It was seen that a fully depleted device can also operate as almost fully depleted or partially depleted (Fig. 4a) [9], and thereby create a neutral region disposed in the channel.

4. Conclusions

The study of different front and back gate biases showed three distinct regimes of conduction: front, back and silicon (Si) volume conduction in Ultra-Thin Buried Oxide SOI MOSFET Devices and this effect is due to charge inversion in the channel when different bias is applied.

Acknowledgments

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Low-Frequency Noise in Inversion Mode Field Effect Nanowire transistors with dimensions reductions

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Abstract

This work presents the low-frequency noise (LFN) investigation in fully depleted (FD) inversion mode (IM) n-FET nanowire MOSFETs (NWFETs) with 50 parallel fins and single fin with W_{fin}=20nm, 45nm, 65nm and 105nm and channel length (L=1µm and 10 µm). Several over drive voltages were applied (V_{GT}=0mV to 200mV in 50mV steps) and (V_{GT}=200mV to 800mV in 200mV steps) with devices working in a linear region (V_{DS}=50mV). The results obtained in a single fin NWFETs with L=1µm and W_{fin}=20nm showed a decrease of spectral noise density (S_{VG}) with V_{GT} increase for frequencies bellow 1KHz. This increase is due to mobility variation (Δµ) at the power spectrum density noise (PSD). It was also possible to see in this device that the generation and recombination noise (g-r) with a decay of $1/f^2$ overlaps the $1/f^{\gamma}$ noise for frequencies above 1KHz. The γ factor changed with V_{GT} (from 1.3 to 0.9) that shows a changing of noise mechanisms from into the depletion region to Si/ HfSiON surface. The normalized noise (S_{ID}^2/I_{DS}^2) behavior with dimensions reduction (W_{fin}) was also observed and showing a good agreement with Δn and Δµ theories.

Keywords—nanowire, n-FET, fully-depleted (FD), low-frequency noise (LFN), inversion mode (IM).

1. Introduction

As technology advances, it suggests the need for new technologies to obtain a higher density that brings less costs, smaller devices and less lower power consumption. The multi-gate transistors such nanowire field effect transistor (NWFETs) in SOI substrates has emerged as an excellent alternative for the reduction of transistors dimensions and power consumption due to good electrostatic coupling that allows a better channel charges control [1].

2. Measurements

The Low-Frequency Noise (LFN) measurements were performed in fully depleted nMOS with 50 parallel fins and single fin inversion mode field effect nanowire transistors NWFETs built in a SOI wafer with L (10µm and 1 µm), W_{fin} (20nm, 45nm, 65nm and 105nm). The gate stack is composed of HfSiON/TiN with EOT=1.4nm, silicon thickness H_{fin}=11nm, intrinsic active layer doping=$1.10^{15}cm^{-3}$ and buried oxide=145nm. The cross sections of these devices can be seen in [2].

A. DC Measurements

Fig. 1. Presents I_{DS}/W_{ef} as a function of the V_{GT} (left axis) where W_{ef} = ($2H_{fin}+W_{fin}$), $V_{GT}=V_{GF}-V_{TH}$, V_{GF} is the voltage applied at gate and V_{TH} is the threshold voltaje. The devices used at the measurements has a L=10µm and 50 fins channel length. Transconductance (g_m/W_{ef}) as a function of V_{GT} is showed at right axis.

The V_{TH} obtained was obtained by second derivation method.

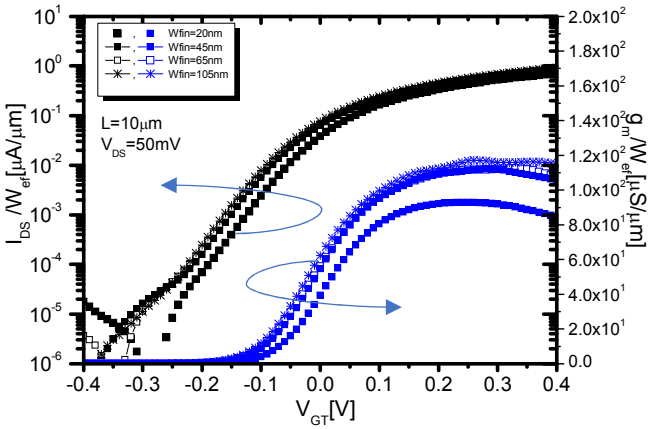

Fig. 1. I_{DS}/W_{ef} as a function of the V_{GT} with W_{fin}=20nm, 45nm, 65nm and 105nm, L=10µm (left axis) and Transconductance (g_m) as a function of V_{GT} (right axis).

B. Noise measurements

Fig. 2. Shows the input referred noise power spectral density (S_{VG}) as a function of frequency with V_{GT} ranging from 0 to 200 mV in a single fin device with L=1µm, with W_{fin}=30nm and working in a linear region with V_{DS}=50mV. For frequencies smaller than 300Hz, the LFN has a $1/f^{\gamma}$ decay and a decrease of the noise with V_{GT} increase. It is possible to see the changing of curve inclination with V_{GT} γ=1.3 for V_{GT}=0 and γ=0.9 for V_{GT}=800mV. The factor "γ" indicates if the traps are inside the gate dielectric, near interface or into the depletion region. For $\gamma \leq 1.0$, the traps are usually within the gate dielectric whereas for $\gamma > 1.0$ most traps are located in the depletion region [3]. In this case, the trapping and detrapping mechanism is coming out from into the depletion region and going to Si/HfSiON surface.

Above 1KHz, all the curves change the inclination that means a translation from $1/f^{\gamma}$ noise to generation and recombination noise (g-r) that has a decay of $1/f^2$. For frequencies above 1KHz is also possible to see that the noise increase with V_{GT} that means a mobility interference in the noise.

Fig. 3. Shows the normalized noise $S_{ID}.W_{fin}.L/I_{DS}^2$ as a function of I_{DS}/W_{fin} for a 50 fins nanowire transistors with L=10µm and W_{fin}=20nm, 45nm, 65nm and 105nm. In this picture is possible to see the noise increase current above 4.10^{-7}A/µm for W_{fin}=20nm and 45nm. It happens due to strongly influence of series resistance [3]. A way of verify the noise origin is from Δn (number carries fluctuation [4]) or Δµ (mobility fluctuatin [5]) is if both S_{ID}/I_{DS}^2 and $(g_m/I_{DS})^2$ curves reduce similarly with the I_{DS} increase, the noise is associated to the carrier number fluctuations, otherwise it is related to the mobility fluctuations [6]. It is possible to see in fig. 3 for drain current bellow 4.10^{-7}A/µm, a weak similarly between curves of S_{ID}/I_{DS}^2 and $(g_m/I_{DS})^2$ that means a mobility fluctuatin interaction on the noise.

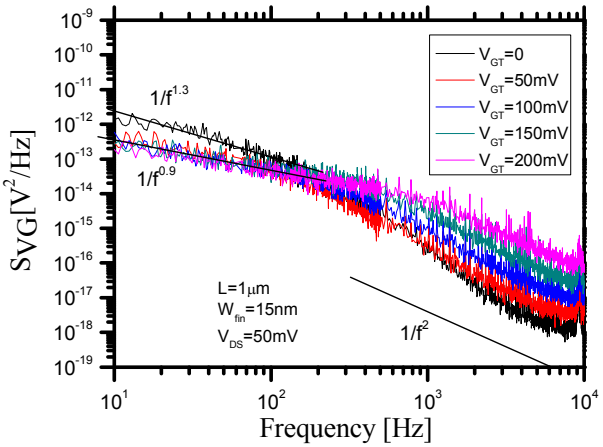

Fig. 2. Input referred noise power spectral density (S_{VG}) as a function of frequency with V_{GT} ranging from 0 to 200 mV with L=1µm and W_{fin}=15nm.

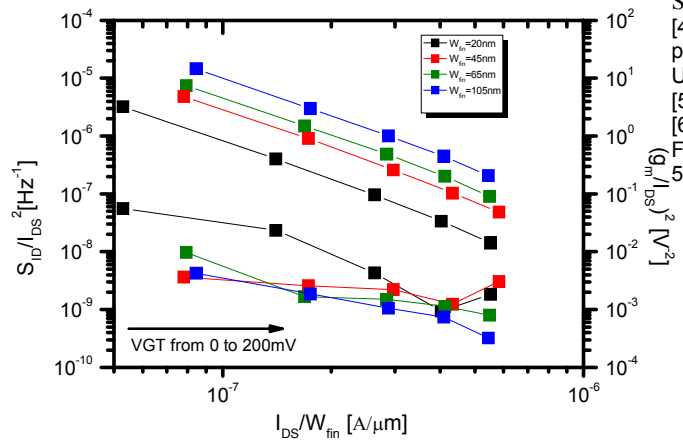

Fig. 3. Curve of normalized current density noise S_{ID}/I_{DS}^2 as a function of I_{DS}/W_{fin} (left axis) and (g_m/IDS^2) as a function of V_{GT} (right axis).

4. Conclusions

This work presented the noise behavior in fully depleted inversion mode (IM) nanowire transistors with several W_{fin} (15nm, 20nm, 45nm, 65nm and 105nm) with 50 parallel fins and single fin with channel length (L=1µm and 10µm) working in a linear region with V_{DS}=50mV.

The noise measurements, the S_{VG} as a function of frequency with V_{GT} ranging from 0 to 200 mV in a single fin device with L=1µm, W_{fin}=15nm with V_{DS}=50mV showed a decay of $1/f^{\gamma}$ for frequencies bellow 100Hz and the γ changing from γ=1.3 for V_{GT}=0 and γ=0.9 for V_{GT}=200mV that indicates the trapping and detrapping mechanism is changing from into the depletion region and going to Si/ HfSiON surface. Above 1KHz, all the curves change the inclination due to a translation from $1/f^{\gamma}$ noise to $1/f^2$ noise. It was possible to see in these curves, the mobility dependence at the LFN.

At the normalized noise S_{ID}/I_{DS}^2 as a function of I_{DS}/W_{fin} for 50 fins nanowire transistors with L=10µm and variable W_{fin} it was possible to see an increase of the noise for current above 4.10^{-7}A/µm for W_{fin}=20nm and 45nm due to strongly influence of series resistance. It was possible to see as well comparing the $S_{ID}.W_{fin}.L/I_{DS}^2$ with g_m/I_{DS}^2 as a function of I_{DS}/W_{fin} the strong mobility influence at the noise.

Acknowledgments

The authors of this work would like to thank CAPES, CNPq and FAPESP for the financial support.

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Influence of Single Event Effects on Breakdown Voltage of Power MOSFETs

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1. Abstract

This paper aims to study the Single Event Upset in power MOSFET transistors when subjected to radiation, as a continuation of a first study entitled "Study of breakdown voltage in Power MOSFETs in harsh Environments". This work investigates the influence of particles radiation in Power MOSFET breakdown voltage. The radiation beam emission in MOSFET structure causes the generation of electron-hole pairs and, for consequence, a transient effect occurs in the drain current, which showed strong dependence on temperature and carriers lifetime. This work studies the behaviour of the drain current transient according to the temperature and the carrier's lifetime, with the variation of the position and the angle of incidence of the radiation beam.

2. Introduction

Significant growth in demand for solutions related to power electronic applications has elected the power metal–oxide–semiconductor field effect transistors (MOSFETs) as an alternative for solid state switching device in DC-AC converters and in power supplies, thanks to their low conduction loss, high input impedances and high switching speed capabilities [1].

The device behaviour depends on the environmental conditions, as operation temperature variation and radiation exposure. Device failures can occur due to continuous exposed to radiation environment, when occur accumulation of loads in the interface, denominated total dose effects [2] or a high energy particle penetrates the structure and may cause transient effects (SEE) [3]. Single Event Upset (SEU) occurs by the penetration of an energetic particle within a device, when occur this penetration, a plasma track is produced along the device, then a electron-hole pairs are generated [4].

The motivation for this work is to investigate the influence of Single Event Upset in power MOSFET structure. This study was realized through of the drain current transient behaviour analysis, considering the carriers lifetime and temperature variation.

3. Numerical Simulations

Two-dimensional numerical simulations were performed using the ATLAS simulator [5], including the Boltzmann and Fermi-Dirac statistics, in order to make the results more accurate.

A. Simulation Results

Fig. 1 and Eq.1 shows the maximum value of the drain current transient (I_{DS}), which illustrates this transient with the temperature variation during the blocking mode (V_{GS} = 0V). The behaviour of these current peaks will be analyzed according to the variation of temperature and carriers lifetime, the position and the angle of incidence of the radioactive beam.

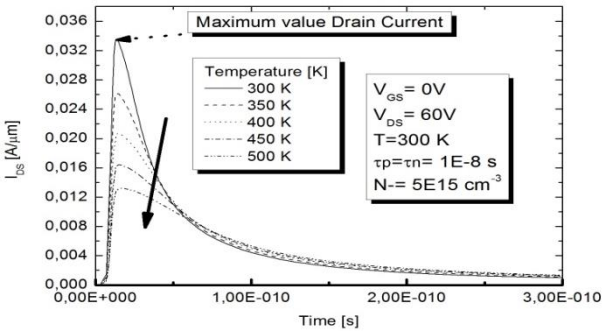

Fig.1. *Transient drain current as a function of time.*

$$I_p(t) = Io.(e^{\frac{-t}{ta}} - e^{\frac{-t}{tb}}) \quad (1)$$

Io is the maximum value of collection loads, *ta* is the time related to the charges collection, *tb* is the time related to the ionization establishment.

Fig. 2 shows the drain current peak behavior according by the change of radiation beam position, with the temperature variation in the range of 300K up to 500K. The first fact observed was the decrease in the peak of the drain current transient with increasing temperature. This fact occurs due to the significant increase in the carriers recombination rate, with the increase in temperature, which causes a smaller number of carriers to be captured by the drain, thus causing a reduction in the drain current. The second fact observed was the increase of maximum value drain current in 1,0μm and 3,0μm.

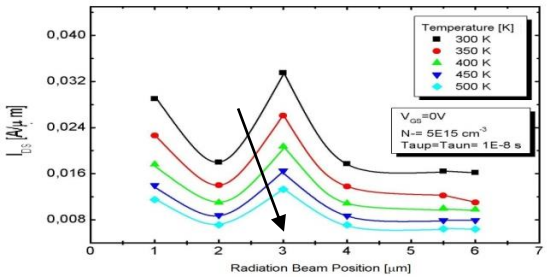

Fig.2. *Maximum value of drain current as a function of position, with temperature variation.*

Fig. 3 shows the drain current peak behaviour, according to the change of radiation beam position, with the carriers lifetime variation in the range of 1.10^{-7}s up

to 4.10^{-7}s. We can see the growth of maximum value in 1,0 μm and a 3,0 μm, it can be explain by the electric field distribution in different regions of the structure. It was note that the drain peak current decrease with the carriers lifetime increase. This can be explain by the drain current behaviour during operation in blocking mode, which is inversely proportional to the carriers lifetime.

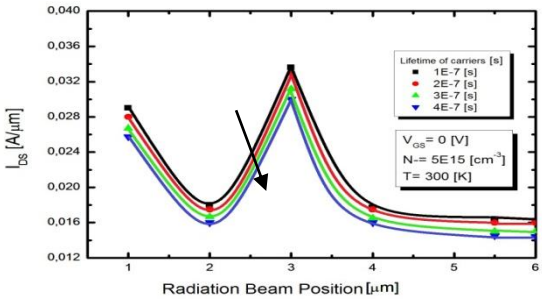

Fig.3. *Maximum value of drain current as a function of position, with carriers lifetime variation.*

Fig. 4 illustrates that for incidence angles from 0 up to 60 degrees, few carriers are captured by the horizontal electric field, resulting in low values of the drain current. For the 90 degree angle the maximum peak of the transient current can be observed, this is due to the smaller distance covered by the incident particle. For angles of 120º to 135º smaller values of drain current were obtained because the distance travelled by the particle was larger, in this way the carrier has more opportunity of recombination before being captured by the drain. With the temperature increase there was a reduction in the transient peak of the drain current for all angles studied.

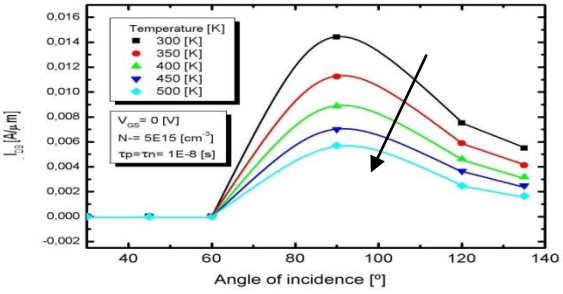

Fig.4. *Maximum value of drain current as a function of incidence angle, with temperature variation.*

According to Fig. 5, a decrease in the peak drain current is observed when the carriers lifetime is increased. Also a growth in the value of the current in the angle of 90 degrees is observed and a decrease in the angle of 120º. This behaviour can be explained by the same reasons discussed earlier.

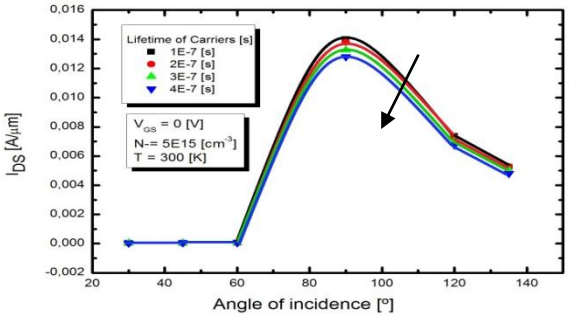

Fig.5. *Maximum value of drain current as a function of incidence angle, with carriers lifetime variation.*

4. Conclusions

By modifying the incidence position of the radioactive beam, the device showed greater sensitivity to the electric field in the regions where the PN junctions are located, because an I_{DS} current of higher value was detected, emphasizing that whenever the beam position change occurred, the behaviour was repeated. It was also noticed a sensitivity to the high temperature, reducing the current values whenever it rises. The lifetime of the carriers influences the transient because when we raise it the current decreases because I_{DS} is inversely proportional to the lifetime. Finally, the behaviour of the transient was analyzed by modifying the angle of incidence of the beam, noting that at 90º the current value is maximum.

Acknowledgments

The authors would like to thanks the Centro Universitário FEI, and CNPq for the financial support.

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Simulation Analysis of Junctionless Transistors with Variable Fin Height

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Abstract

This work presents an analysis of the electric parameters of junctionless transistors for variable fin height. Results shows that for long channel devices double gate structure has more advantages, while for smaller channels the nanowire structure has more promising characteristics.

1. Introduction

Junctionless nanowire transistor (JNT) remains one of the promising structures for the continuous scaling of MOSFETs [1]. This device presents a uniformly and highly doped channel and works with different conduction mechanisms than the common inversion mode nanowire and therefore, presents different behaviors for the different gate structures. The main gate structures used today are the nanowire and the FinFET, both with excellent gate control. The first has a short fin height while the latter has a taller fin height. So, with a variation of this geometrical parameters the device produces different results as the gate structure changes. The increase in fin height shows several advantages with reduced random doping fluctuation [2], increase in the strain by the gate [3] and increase the current without increasing the area of the device while nanowire transistors shows great electrostatic control of the gate and excellent electric parameters [4]. The tradeoffs on the electrical properties of JNT varying the fin height with respect to the fin width are investigated in this work for long and short channel devices.

2. Simulated Devices

The simulated devices are SOI junctionless transistors and have buried oxide thickness of 150nm, equivalent oxide thickness of 1.3nm, fin width (W_{FIN}) of 13nm, channel length (L_G) of 100nm, 50nm and 30nm and variable fin height (H_{FIN}) from 10nm to 60nm, and spacers of 30nm. The devices were simulated using a higher doping on the extensions to reduce the series resistance. The simulation used work function of 4.7eV, and doping of 4.10^{18} cm^{-3}, and the models for bandgap narrowing, generation-recombination with doping dependence, and carrier mobility which consider the transport and scattering mechanisms in the accumulation layer. A good agreement between measured devices and calibrated simulation results from our previous work [5] provide a way to study the influence of the fin height on the electrical characteristics of junctionless transistor.

3. Results

From the devices simulated some parameters were extracted and analyzed in this work, mainly the subthreshold slope, the transconductance, the drain induced barrier lowering, and the on and off current ratio.

Fig. 1 shows the normalized transconductance and the subthreshold slope as a function of the fin height for several channel lengths and Fig. 2 shows the improvement for these two parameters compared to the shortest device with H_{FIN}=10nm for each channel length. From the normalized transconductance we can see a better improvement for the nanowire structures as we decrease the fin height, this tendency occurs for all channel lengths. We can see that for the normalized transconductance, the degradation of increasing the fin height gradually increase and goes up to 16% for long channel devices and up to 12% for short channel ones, with the L_G=50nm goes up to 14% at H_{FIN}=60nm. For the higher transconductance, and therefore the mobility, for smaller fin height can be attributed to the reduced Coulomb scattering of electrons at the accumulation regions of conduction [6], having a similar effect as the reduction of the channel width.

For the subthreshold slope, the distinction between short and long channel length can be seen, the increase in the fin height provides a better slope to longer channel devices and while for short channel ones the nanowire devices have a better improvement as the fin height becomes smaller. The subthreshold slope variation is very small, and for long channel devices the increase in the fin height is up to 4%, the same tendency for L_G=50nm with a maximum improvement at H_{FIN}=60nm of 3%, while for the short channel ones the degradation from increasing the fin height is higher for

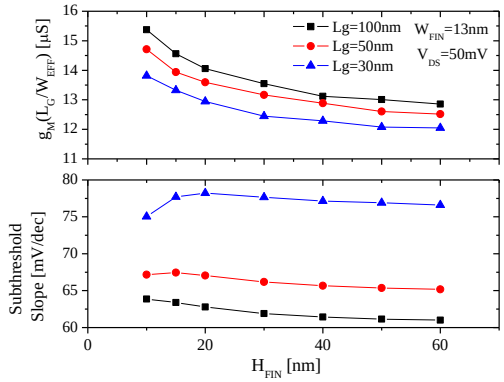

Fig. 1. *Normalized Transconductance and Subthreshold slope as a function of the fin height.*

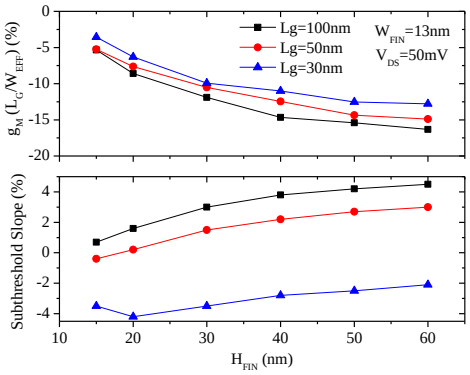

Fig. 2. *Percentage improvement with reference to the smaller fin height (10nm) for each channel length for normalized transconductance and Subthreshold Slope.*

H_{FIN}=20nm with 4% and for H_{FIN}=60nm the degradation goes down to around 1%. This decrease on the subthreshold slope for long channel devices can be attributed to the reduced body factor of the device, accounted by the model in [7]. For smaller channel lengths the effects of the short channel effects become greater than the effect from the body factor and the tendencies changes.

Fig. 3 shows the DIBL and the I_{ON}/I_{OFF} ratio of the device as a function of the fin height and Fig. 4 shows the improvement for these two parameters compared to the shortest device with H_{FIN}=10nm for each channel length. From these curves we can see that the improvement from the DIBL comes from reducing the fin height for all channels, although the DIBL is already small for long channel devices the increase in fin height degrades the DIBL up to 20% at H_{FIN}=40nm and it improves a little as the fin height goes up to 60nm to 15%. The L_G=50nm follows the tendency of L_G=100nm really close with a slight increase on the degradation as the H_{FIN} increase. For the short channel devices this degradation increases for up to 45% for H_{FIN}=60nm. The better improvement from the nanowire device, shows a better electrostatic control of the gate, reducing the influence of the short channel effects on this device.

For the I_{ON}/I_{OFF} ratio we can see almost no variation on this parameter after H_{FIN}=30nm for all channel lengths, and at smaller fin height for long channel devices there is a decrease in the I_{ON}/I_{OFF} ratio with the

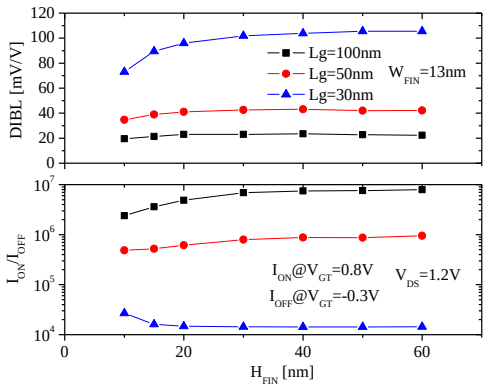

Fig. 3. *DIBL and I_{ON}/I_{OFF} ratio as a function of the fin height.*

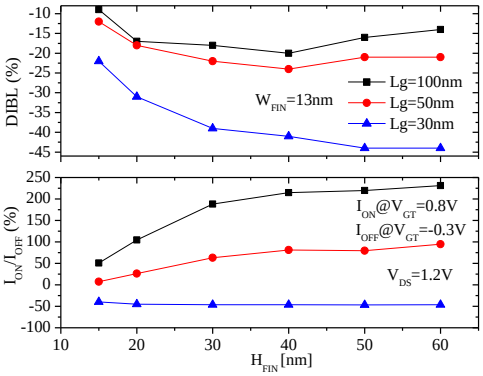

Fig. 4. *Percentage improvement with reference to the smaller fin height (10nm) for each channel length for DIBL and I_{ON}/I_{OFF} ratio.*

same effect for the L_G=50nm. But as the channel length decreases we see the improvement for short fin height. For long channel (L_G=100nm) the improvement from increasing the fin height goes up to 236%, while for L_G=50nm it goes up to 96%. And for short channel devices the degradation as we increase the fin height goes up to 46%. This result is mainly affected by the off current (and therefore the subthreshold slope) that is much smaller in long channel devices, compared to smaller channel ones.

4. Conclusions

In this work several electrical parameters were analysed and for the nanowire gate structure short channel devices produces DIBL 45% lower and transconductance 12% higher compared with taller fin height, while for FinFET like structures better parameters like subthreshold slope improve up to 4% and I_{ON}/I_{OFF} ratio up to 236% for long channel devices compared with the smaller fins.

Acknowledgments

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Implementation of Long Channel Triple-Gate Junctionless Nanowire Transistor Analytical Model in VERILOG-A

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1. Abstract

This paper shows the results of a VERILOG-A implementation for junctionless nanowire transistor on long channel device. The implementation was written for usage with SPICE simulators, allowing the projects of circuits with this device.

2. Introduction

Junctionless nanowire transistors (JNTs) have been proposed as an alternative for the sub–20nm era simplifying the fabrication process [1]. JNTs are multi–gate devices generally fabricated in silicon–on–insulator (SOI) substrates, providing better electrostatic control of channel charges due the presence of gate on more sides of silicon strip [2]. A schematic view of the JNT is shown in fig. 1, where the silicon width (W) and height (H), the gate oxide and buried oxide thickness (t_{OX} and t_{BOX} respectively) and channel length (L) are indicated.

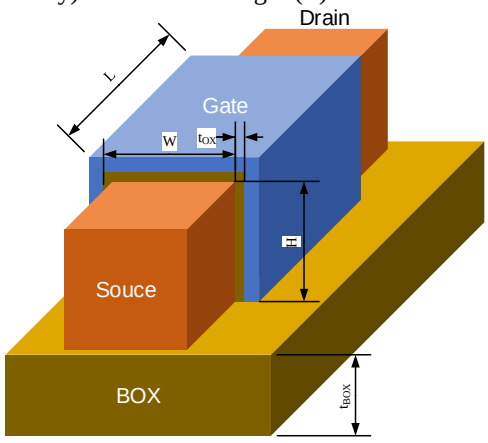


Fig.1. *Schematic View of a JNT.*

A JNT has constant doping profile (constant type and concentration) from source to drain, simplifying the fabrication process. The off state in JNTs is obtained by full depletion of the silicon layer on the channel, related to the workfunction difference between the gate and the silicon film [3]. For an n-type JNT the gate voltage increase reduces the depletion depth allowing a neutral path for current flow between source and drain (I_{DS}). Further increase to the gate voltage (V_{GS}), larger than the flatband voltage creates an additional current component associated with the accumulation layer at the interfaces.

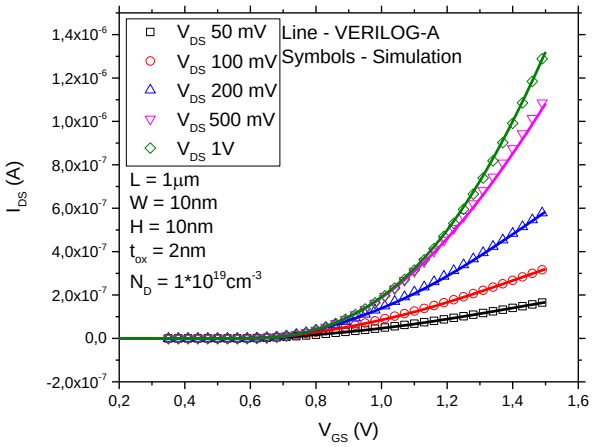
The model which was implemented in VERILOG-A, is based on the difference of surface potentials in source and drain [4].

3. Result and Discussions

The analytical model has been implemented in VERILOG-A, the *de-facto* standard language for defining compact models [5] and tested with ELDO simulator from Mentor Graphics [6]. For validation of results, the implementation was compared with tridimensional numerical simulations obtained from Sentaurus Devices program [7]. The models used for Sentaurus numerical simulations accounted for are Phumob (Philips Unified Mobility Model), Lombardi, Canali, Shockey-Read-Hall Recombination, BandGapNarrowing and Density Gradient Quantization Model.

The long channel analytical model has been implemented following the work of Trevisoli et. al [4]. The model has been encoded in VERILOG-A language and the simulations where executed using SPICE environment in observance of the simulator limitations for long channel transistors.

The figure 2 shows the I_{DS}xV_{GS} with several drain bias voltages (V_{DS}) in linear (A) and logarithmic (B) scales of JNT comparing VERILOG-A implementation with numerical simulations.



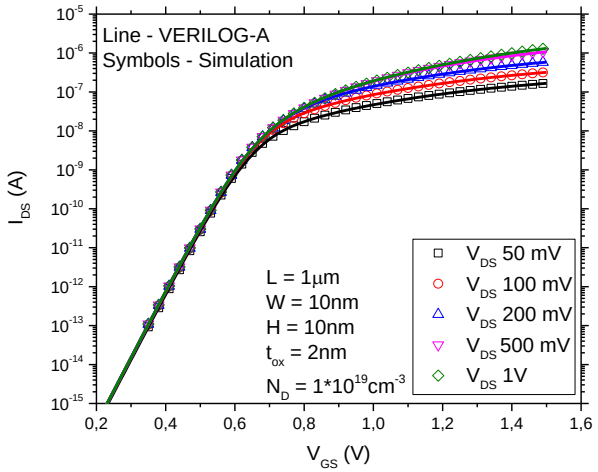


Fig.2. *$I_{DS}xV_{GS}$ Curve of JNT.*

The results of figure 2 show good agreement between the implemented model in VERILOG-A and the numerical simulations for any V_{DS} bias in both subthreshold and above threshold regions. The maximum error for the drain current is 14,5% at V_{DS} of 50 mV and V_{GS} around V_{Th}.

The g_MxV_{GS} curve shows similar behaviors when compared with the simulations. Fig. 3 shows the g_MxV_{GS} curves with various V_{DS} of JNT comparing the implementation with simulations.

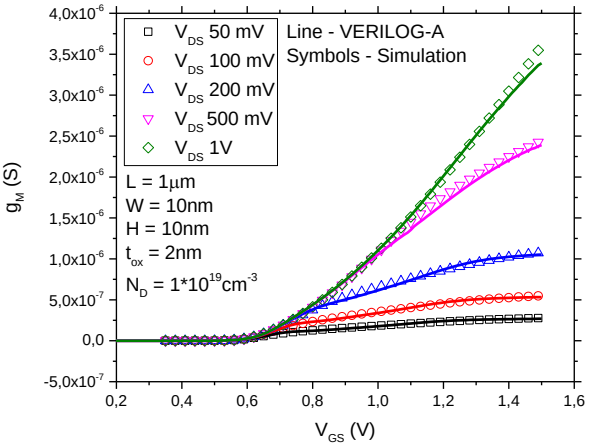


Fig.3. *g_MxV_{GS} Curve of JNT.*

As for the I_{DS} curves, the transconductance is well described by the model implementation in any gate and drain voltage. The maximum error obtained in this analysis is 16,9% with V_{GS} around V_{Th}.

The fig. 4 show $I_{DS}xV_{DS}$ curves obtained at several gate voltage overdrives ($V_{GT}=V_{GS}-V_{Th}$, V_{Th} being the threshold voltage) of JNT.

In $I_{DS}xV_{DS}$ curves, with the same set of parameters, the error obtained is less than 4%.

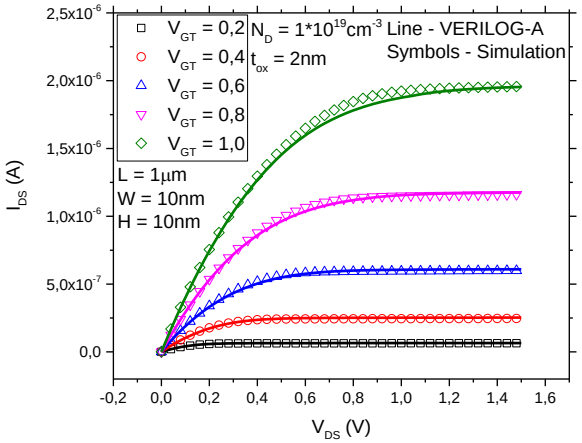


Fig.4. *$I_{DS}xV_{DS}$ Curve of JNT.*

4. Conclusions

The analytical model for long channel JNT has been successfully implemented in VERILOG-A language and devices characteristic curves where obtained using SPICE simulator. The comparison between SPICE simulated curves and tridimensional numerical simulations showed good agreement for the drain current and its derivatives with a maximum error of 16,9%.

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A temperature independent current reference for 1V supply voltage

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1. Abstract

This work presents a BandGap reference current generator, a circuit designed to provide a constant 20µA reference current independent of the operation temperature, in the range of -40°C to +125°C. The current generator circuit was designed using a commercial CMOS Technology TSMC 180nm, provided through the Europractice mini@sic program.

2. Introduction

Many analog integrated circuits requires a stable current to bias its circuits in the proper operation point or to serve as an element of reference (e.g. operational amplifiers and current steering digital-to-Analog converters). Usually, this reference current is distributed to the analog blocks using current mirrors, reasons why a reliable reference current, independent of the supply voltage and operation temperature, is desirable. A popular way to generate an independent reference current is through the classical Voltage to current (V-I) [1] converter as shown in Fig.1.

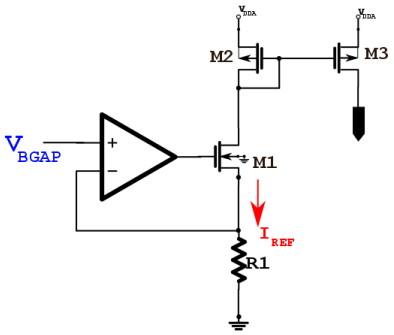

Fig. 1 – Classical V to I converter

The V_{BGAP} input reference voltage generally is provided through a BandGap voltage generator. This topology works well, but, as the supply voltage decreases, the size of the current mirror formed by M2 and M3 demands care and may compromise the stability of the system, also the V_{BGAP} must decreases. In order to avoid these issues, a current reference could be generated directly from the BandGap generator, without a reference voltage.

The topology, shown in Fig 3., provides a reliable 20µA reference and a current proportional to the absolute temperature PTAT [2] for a supply voltage over 1V. The circuit is designed to be used in a temperature sensor, under development by our research group, but the IP block can be used as current generator in many other applications.

3. Principle of Operation and Design

Two currents with opposite thermal behavior are added in order to cancel out the temperature changes. A current which is proportional to the absolute temperature (PTAT) and a complementary current, which decreases with temperature (CTAT), are combined to get a compensated current, as shown in Fig. 2.

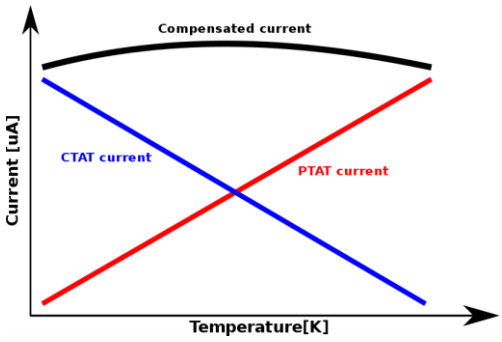

Fig. 2 – Temperature behavior of the two used currents

A schematic of the design is shown in Fig.3. The CTAT current is generated through the V-to-I Converter (formed by the OTA1, Resistor R_1 and MOSFET M_1), which converts the base-emitter voltage of the bipolar transistor Q1 into a current. For the PTAT current, the core of the classic BandGap circuit is used, which provides a current proportional to the temperature, found from the difference of base-emitter voltage of the bipolar transistors Q1 and Q2(they have two different junction areas). Note that both current generators share the bipolar transistor Q1, which reduce the number of required devices. The equations for both currents are:

$$\Delta V_{EB} = \Delta V_{EB1} - \Delta V_{EB2} \qquad (1)$$

$$I_{CTAT} = \frac{\Delta V_{EB1}}{R2} \qquad (2)$$

$$I_{PTAT} = \frac{V_T \ln(N)}{R1} \qquad (3)$$

Where, V_T is the thermal voltage, N the proportion between the junctions and V_{EB} the base-emitter voltage.

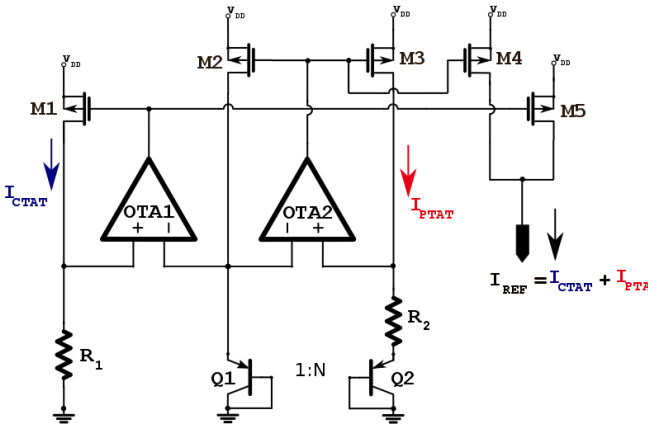

Fig. 3 - Circuit used to generate a reference current independent of temperature. (start-up circuit not shown)

A sum of both currents is made through current mirrors made by M4 and M5. This strategy is similar to that used on the classical BandGap reference circuit [3], the main difference is that all the attention is given to the current generation and compensation. Since CTAT and PTAT current changes in different rates, in order to shape the compensated current I_{REF}, both currents should be multiplied by proportional factors, as shown in the follow equation (4):

$$I_{REF} = \alpha I_{CTAT} + \beta I_{PTAT} \qquad (4)$$

Where α and β are the related slope terms of both currents, CTAT and PTAT. The transistors M4 and M5 are also responsible to adjust them, through the equations (5) and (6).

$$\alpha = \frac{(W/L)_{M5}}{(W/L)_{M1}} \qquad (5)$$

$$\beta = \frac{(W/L)_{M4}}{(W/L)_{M3}} \qquad (6)$$

4. Simulation results

The topology presented on Fig. 3 has been designed for the TSMC 180nm CMOS technology, the specification of current was 20uA. The design parameters are $\alpha = 1{,}2$; $\beta = 0{,}8$ and $N = 8$. The deviation in a range of -40°C to +125°C was around 1%.

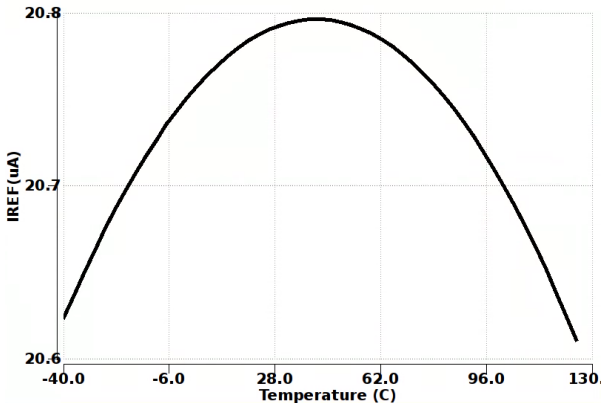

Fig. 4 – Dependence of current reference on temperature

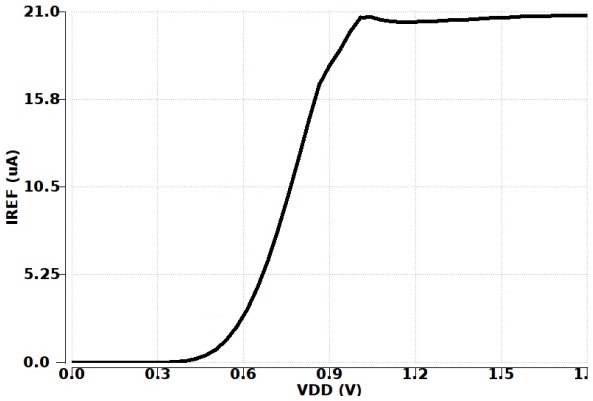

Fig. 5 – Current reference against supply voltage

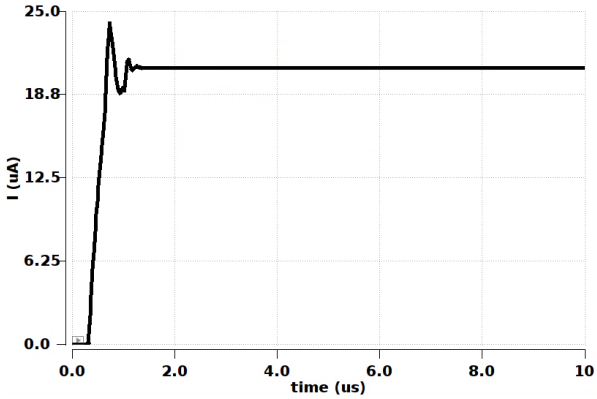

Fig. 6 - Current reference start up time for a supply voltage ramp of 1us

5. Conclusions

We have implemented a 20µA reference current generator, which works up to 1V supply voltage using the TSMC 180nm technology. The circuit shows a stable current output with temperature, with a simulated deviation around 1%. The circuit is simple to implement and can be used in a variety of applications, in our case, it is intended to be used as core of a CMOS integrated temperature sensor.

Acknowledgments

The authors wish to thank Europractice through mini@sic program for the integration and Prof. Luis Carlos Kretly for the support of IC fabrication.

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EXPERIMENTAL EVALUATION OF MISMATCHING OF GC SOI MOSFETS

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1. Abstract

This paper presents an experimental study of mismatching on the analog characteristics of fully-depleted graded-channel SOI MOSFET in comparison to uniformly doped transistors. Using structures fabricated at the same chip and with the same technology, important parameters are analysed, such as threshold voltage, transconductance, Early voltage and etc.

2. INTRODUCTION

Graded-Channel SOI MOSFET (GC) presents asymmetric doping concentration along the channel [1], which is divided in two regions: the first region is highly doped (HD), it is near the source region and is responsible for fixing the threshold voltage of the device; the second region is lightly doped (LD), the remaining channel length is kept with the natural wafer doping concentration, acting as an extension of the drain region. The GC's effective channel length is practically the length of the highly doped region while in saturation (L_{eff}=L-L_{LD}, being L the channel mask length and L_{LD} the lightly doped channel length).

Several papers report advantages of GC SOI devices in comparison to uniformly doped devices, such as increase of drain current (I_{DS}), transconductance (g_m), Early voltage (V_{EA}) and decrease of drain output conductance (g_D) [2, 3].

In this work an experimental evaluation of the mismatching of GC SOI MOSFETs is presented, focusing on analog parameters, such as transconductance in saturation, output conductance, intrinsic voltage gain and Early voltage. Differently of the previous works in [4, 5] this study has been carried out with dedicated structures designed for mismatch evaluation minimizing the number of external variations influencing the measured data.

The studied devices structure and characteristics can be found in [6].

3. EXPERIMENTAL RESULTS AND DISCUSSION

The I_{DS} *versus* V_{GF} and I_{DS} *versus* V_{DS} curves were measured, the effective L_{LD}/L ratio for each device has been experimentally obtained according to the method described in [1] and the mean effective L_{LD}/L and standard deviation are presented in Table I. As can be noted, the standard deviation in the extracted L_{LD}/L increases as the ratio is raised, and the subthreshold slope values are close to the physical limit of 60 mV/dec at room temperature, showing that no important degradation due to short-channel effects has occurred.

TABLE I. SUBTHRESHOLD SLOPE EXTRACTED FROM THE MEAN CURRENT CURVES.

L_{LD}/L		S_{mean} [mV/dec]
mask	*effective*	
0.000	–	63
0.250	0.264 ± 0.0200	64
0.375	0.393 ± 0.0347	66
1.000	–	68

The threshold voltage (V_{TH}) has been extracted for each device using the double derivative method [7]. The obtained mean threshold voltage ($V_{TH,\ mean}$) and its standard deviation (σV_{TH}) are presented for the four different arrays of devices, and the resulting values are presented in Table II.

TABLE II. MEASURED MEAN THRESHOLD VOLTAGE AND THRESHOLD STANDARD DEVIATION.

L_{LD}/L		$V_{TH,\ mean}$ [mV]	σV_{TH} [mV]	$\sigma V_{TH}/V_{TH,\ mean}$ [%]
mask	*effective*			
0.000	–	104.89	6.45	6.15
0.250	0.264 ± 0.0200	127.53	7.93	6.21
0.375	0.393 ± 0.0347	105.26	7.22	6.86
1.000	–	-596.50	12.40	2.08

As can be noted, the mean V_{TH} values for GC devices are close to that presented by uniformly doped transistors with HD channel. Also, the relative standard deviation shows a slight worsening when the GC structure is used, which is related to the channel length reduction as the L_{LD}/L is increased and the larger standard deviation of L_{LD}/L ratio definition, as seen in the results shown in Table I.

According to [8], the relative mismatch in the drain current can be expressed as a function of the mismatch in the threshold voltage and current factor $\left(\beta = \mu_{eff} C_{ox} \frac{W}{L}\right)$, as shown in equation (1), where μ_{eff} is the effective carrier mobility and C_{ox} is the front gate oxide capacitance per unit area.

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{-\Delta V_{TH}}{V_{GF} - V_{TH}} + \frac{\Delta \beta}{\beta} \quad (1)$$

Table III presents $g_{m,mean}$ and $\sigma g_m/g_{m,mean}$ for all devices biased at V_{GT} = 200 mV and V_{DS} = 1.5 V. These results show that the standard deviation is worsened in GC devices with

same gate L (due to variations in the current factor) but it is only slightly higher in then uniformly devices, since the mean value is increased by the reduction of effective channel length.

TABLE III. MEASURED MEAN TRANSCONDUCTANCE AND TRANSCONDUCTANCE STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$g_{m,\,mean}$ [µS]	σg_m [µS]	$\sigma g_m/g_{m,\,mean}$ [%]
Mask	*effective*			
0.000	–	141.00	5.98	4.23
0.250	0.264 ± 0.0200	203.00	9.03	4.44
0.375	0.393 ± 0.0347	257.00	12.66	4.91

Table IV presents the $g_{D,mean}$ and $\sigma g_D/\sigma g_{D,mean}$ were extracted at V_{GT}=200 mV and V_{DS} = 1.5 V. Contrarily to the results obtained for g_m, the relative standard deviation of g_D is worse when the graded-channel structure is used, despite of the smaller σg_D presented by GC devices in comparison to the uniformly doped transistor.

TABLE IV. MEASURED MEAN OUTPUT CONDUCTANCE AND STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$g_{D,\,mean}$ [S]	σg_D [S]	$\sigma g_D/g_{D,\,mean}$ [%]
mask	*effective*			
0.000	–	1.47×10^{-6}	97.6×10^{-9}	6.63
0.250	0.264 ± 0.0200	0.27×10^{-6}	31.9×10^{-9}	11.6
0.375	0.393 ± 0.0347	0.22×10^{-6}	27.5×10^{-9}	12.4

The Early voltage ($V_{EA}=I_{DS}/g_D$) has been extracted for each device, the resulting relative deviation has shown to be reduced in the entire V_{DS} range as can be seen on Figure 1.

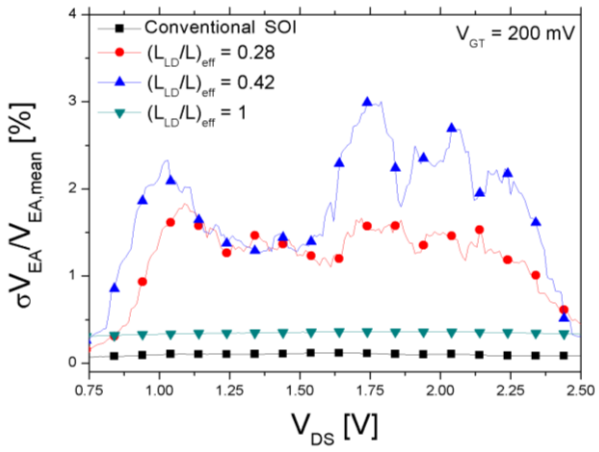

Fig. 1. *Early voltage relative deviation as a function of the drain current with V_{GT}=200mV.*

Finally, the intrinsic voltage gain ($A_V=g_m/g_D$) has been obtained at V_{GT}=200 mV and V_{DS}=1.5 V for each device in order to evaluate the mismatch. Table V shows that $A_{V,mean}$ increases when L_{LD}/L rise, but there is also a worsening of matching. Although there is an increase in the $\sigma A_V/A_{V,mean}$, the maximum value is in the order of those obtained for $\sigma g_D/g_{D,mean}$ indicating the larger source of mismatch in GC SOI with longer L_{LD} is associated with the mismatch in g_D.

TABLE V. MEASURED MEAN GAIN AND GAIN STANDARD DEVIATION AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$A_{,\,mean}$ [V/V]	σA [V/V]	$\sigma A/A_{,\,mean}$ [%]
mask	*effective*			
0.000	–	95.99	3.94	4.11
0.250	0.264 ± 0.0200	744.75	73.99	9.93
0.375	0.393 ± 0.0347	1174.63	130.36	11.09

CONCLUSIONS

This paper presents an experimental evaluation of the mismatching effects on analog parameters of GC SOI transistors. Results show that the relative mismatching of GC devices analog characteristics are higher than the conventional transistor. The standard deviation of drain current on GC devices is also slightly higher. The measured mismatch on the output conductance is larger compared to the transconductance mismatch while the device is operating on the region of interest for analog applications. This larger deviation of the output conductance is transferred to the voltage gain leading to similar mismatch in the latter.

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Design of a Customized Microcontroller Focusing on Task-Based Systems

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1. Abstract

The use of Field Programmable Gate Array (FPGA) [1] is a common practice for the design of complex digital systems, especially when solutions based on microcontrollers or microprocessors become inefficient in terms of the software performance and limited clock speed. Since the FPGAs are based on the arrangement of programmable hardware blocks, it is possible to use the parallel processing approach aiming the design of different synchronous and asynchronous functions. In this context, a FPGA is used to validate a new architecture for microcontrollers, called Interlocked Hardware Microkernel (IHM) Plasma (IHM-Plasma). It was specialized designed to boost de processing performance of task-based systems. In this context, the Plasma Central Processing Unit (CPU) was modified incorporating new functional blocks to it is able to perform the function of the scheduler that usually is made by software. Remarkable results were obtained in terms of time reduction to perform the task switching and to decide the next task to be run. After the validation of this innovative IHM-Plasma CPU in FPGA, the Electronic Design Automation (EDA) tools from Cadence [2] was used to generate its layout file (GDSII), aiming its later manufacture.

2. Introduction

The use of the programmable logic devices, such as FPGAs to design customized digital electronic systems, named “soft hardware”, is advantageous for prototypes, small volumes of production, etc. On the other hand, the development of an ASIC is the natural pathway when are required high production volumes, and low-cost. The ASICs are designed for specific scopes and do not demand extra components that will not be used, in contrast of the FPGAs. Table I represents the relationship between the FPGA and digital ASIC design in terms of the development and production costs. Although a design implemented with FPGA be relatively cheap, it has a high production costs, in contrast to the ASIC, regarding high production volumes [3].

Table I. *The project and production costs of a CMOS IC by using a FPGA and ASIC.*

Device	***Project***	***Production***
FPGA	low	high
ASIC	high	low

In this context, the main objective of this paper is to describe the advantages of a new microcontroller architecture to be used in task-based systems, such as those related to the real-time operating system (RTOS). The proposed microcontroller is based on a 32-bit Plasma CPU [4]. This architecture was changed to encompass new functions to make feasible the implementation by hardware of the scheduler used in the microkernel of the task-base systems (hardware scheduler, a tasks dispatcher, and a mechanism to handle periodic tasks, etc.) [5]. The innovative microcontroller based on the Plasma CPU was named IHM-Plasma (Interlocked Hardware Microkernel-Plasma) [6]-[7]. The secondary objective is show the flow to convert the FPGA design into a ASIC layout. In order to manufacture the IHM-Plasma for future characterization.

3. IHM-Plasma architecture

The IHM-Plasma is an innovative microcontroller architecture which is responsible for performing the tasks sequencing and dispatching needed in the task-based systems, such as those that using RTOS. The tasks can be defined as an instance of a function (thinking on the C language) and is characterized by a context (system variables to be controlled). In task-based system, an execution of a task can be interrupted by the CPU and after another task can be run by the CPU. The microkernel controller is responsible for this. Besides, the scheduler is responsible for deciding what is the next task will be run. This is done by software through an algorithm (microkernel). When the scheduling is preemptive, as in this case study, a task can be interrupted before completing its execution, aiming to share the CPU processing time with the other tasks to be run. In order to avoid conflicting and data overwriting in the memory, each task has a separate memory block which is responsible for storing the contents of the stack, etc. and also another block called Task Control Block (TCB) that stores the context and other important information about task features.

One bottleneck of these systems is the time taken to perform the context switching. During this process, the CPU is busy saving the internal registers and the PC in the corresponding TCB and coping data from the next task TCB to the IRB and the PC. This project proposes the creation of another IRB that works in parallel to the other. While one is being used by the CPU to run a task, the other is being used by the IHM the prepare or save the context in the correct TCB. This way, when is time the change the running task, the CPU is paused only to invert the IRBs between the CPU and the IHM.

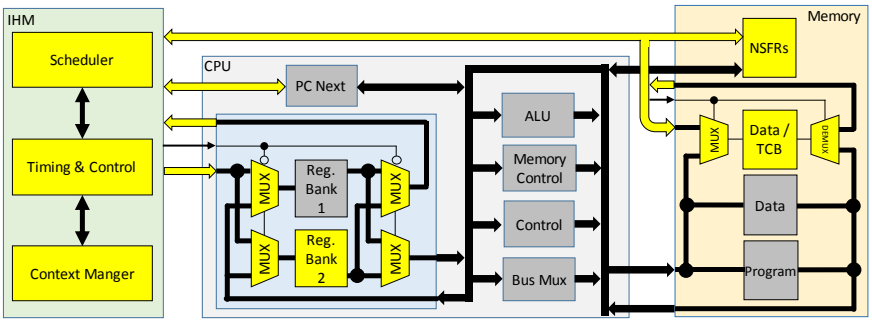

Fig.1. *Simplified block diagram of the proposed IHM-Plasma.*

Table II. *Used resources to implement IHM-Plasma in FPGA and ASIC.*

Block	***FPGA (LUT)***	***FPGA (reg.)***	***ASIC (gate)***
CPU	35%	39%	36%
IHM	53%	30%	48%
Extra IRB	10%	30%	15%
UART	1%	2%	2%

Comparative studies confirmed a reduction on the context switching time from a period of 136 clock cycles to only 2 clock cycles. Another advantage of using the IHM-Plasma is that the scheduling algorithm is executed by hardware, in parallel with the execution of the code by the CPU. This implementation reduces the CPU overhead and improves determinism of the task-based system.

Fig. 1 illustrates the block diagram of the IHM-Plasma architecture. In yellow the blocks that were implemented to make feasible the IHM, New special function registers (NSFR) were implemented to configure and control microkernel functions (software). The IHM is composed by three main blocks: (a) Scheduler: responsible for deciding what is the next task to be run; (b) Context Manager: responsible for dispatching the tasks; (c) Timing & Control: responsible for controlling the operations of the microkernel, generating the synchronism signals sent to the CPU and other IHM blocks. This architecture can handle up to 32 tasks with 8 priority levels and is able to control 8 periodic tasks, without CPU interference.

4. From FPGA to ASIC

The IHM-Plasma was specially designed and tested using an Intel FPGA (Cyclone IV family). The Quartus II EDA was used to implement the hardware blocks by using VHDL. The ModelSim EDA was used to perform the functional simulation of the IHM-Plasma.

When we decide by configuring an FPGA device instead of an ASIC, we ignore many questions like testability of internals blocks, I/O sub-circuits, clock and power consumption distribution, embedded memories, die dimensions, ESD protection, packaging, and so on. Thinking on ASIC implementation, the digital CMOS ICs is based on the VHDL code used for the hardware description, called RTL synthesis model. The following steps were performed to transform the RTL files into a layout: (I) Gate-level: conversion the RTL into gate-level netlist based on technology elements of the desired manufacturing process; (II) Floorplan: defines die size and places the digital blocks regarding a die area; (III) Power: defines power pins, creates power ring and stripes on die area, and route the power signals; (IV) Placement: places the standard cells in each block and pre-routes them; (V) Route: executes the connection between the cells; (VI) Verification: checks the design rules (DRC).

The layout was designed using the commercial 130 nm Silicon-Germanium (SiGe) CMOS ICs manufacturing process from Global Foundries. Table II shows the percentage of resources used (LUTs and registers for FPGA technology, and gates for ASIC implementation) for the IHM-Plasma project, disregarding memory used for data and code. It is observed in both cases that the IHM represents about 50% of the consumed resources.

4. Conclusion

This study presented the IHM-Plasma as an efficient alternative for the processing of task-based systems, where the time to perform a context switch is reduced by 98.5% compared to conventional software approach. In addition, up to 32 tasks can be scheduled without CPU interference.

The proposed microcontroller was implemented in FPGA and converted into an GDSII file to generate the layout. In both cases, the functions of the microkernel correspond to 50% of the resources consumed.

Acknowledgment

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Experimental Comparative Study Regarding the Mismatch Between the FISH nMOSFET and its Conventional Counterparts

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1. Abstract

This paper presents an experimental comparative study of the devices matching regarding a sample of 23 Metal-Oxide-Semiconductor Field Effect Transistors, n-type (nMOSFETs), which were implemented with the FISH and rectangular layout styles, respectively. Considering some relevant electrical parameters studied in the paper, the results indicate that the FISH nMOSFETs with α angle equal to 90˚ can be considered an alternative device to boost about, at least 80% in average, the devices matching, in relation to those observed with the rectangular MOSFET counterparts, considering the same bias conditions.

Keywords: Devices Matching, nMOSFETs, analog CMOS ICs, new layouts of MOSFETs.

2. Introduction

The continued evolution of technologies regarding microelectronics (known as downscaling) and also the layouts of semiconductor devices vastly affects the electrical performance of analog Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) [1-4]. Besides, numerous significant researches improve the electrical performance of the Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs). For instance, new devices structures [5], new manufacturing processes and materials [6] are developed and studied. Currently, an innovative gate geometry was proposed and also developed which is defined as "Interface Engineering between the Drain/Source and Gate Regions", or simply "gate layout changing of MOSFETs", although it is still not commercially used. Furthermore, this new layout technique does not add any extra cost to the electric current and sophisticated Complementary MOS (CMOS) ICs manufacturing processes (such as Bulk, SOI, Ultra-thin body, UTB, and buried-oxide, UTBB, etc.). For example, one of this layout style is the fish shape gate type (also known as FISH MOSFETs, n-type, FnM) (Figure 1). This name was given because if the channel region is observed concerning a three-dimensional (3D) way, through 3D numerical simulation, it is possible to visualize a FISH structure (shape).

By analyzing Figure 1, it is observed that W is the channel width, L is the length of the channel, L_{eff} is the effective channel length (L_{eff} is equal to L / sin (α / 2) [7,8]), α is the angle of the FnM, and $\overrightarrow{E_1}$ and $\overrightarrow{E_2}$ are two longitudinal electric field components generated by the application of V_{DS}, which are perpendicular to the drain / channel interfaces, $\overrightarrow{E_T}$ is the longitudinal electric field which is equal to the sum vector of $\overrightarrow{E_1}$ and $\overrightarrow{E_2}$, which is in the same direction as L_{eff} and the density current [7,8]. It is verified that the design of the FnM makes it possible to increase the L of this type of transistor [7,8], giving rise to the figure of merit $I_{DS}/(W/L)$, which represents the capacity of the transistor to provide a value of the drain current I_{DS} as a function of the aspect ratio W/L [7,8]. Equation 1 illustrates the relation between the drain current (I_{DS}) of the FnMs and the CnMs counterparts.

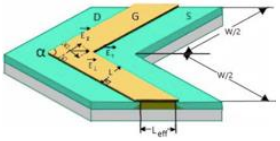

Fig.1 Fish layout style for MOSFETs (also known as FISH MOSFETs, n-type, FnM).

$$\frac{I_{DS_{FnM}}/(W/L)}{I_{DS_{CnM}}/(W/L)} = \frac{I_{DS\_FnM}}{I_{DS\_CnM}} \cdot \left[\frac{1}{sen(\alpha/2)}\right] \geq 1, \text{ for } 0^{\circ}<\alpha<180^{\circ} \quad (1)$$

In Equation (1) I_{DS_FnM} is the drain current of the FnM and I_{DS_CnM} is the drain current of the CnM. It is verified that the FnM produces higher value of $I_{DS}/(W/L)$ when comparing this parameter with the equivalent CnM, taking into account the same bias conditions.

3. Description of the Devices

The FISH nMOSFET devices (FISH nMOSFET, FnM) and the respective Conventional nMOSFET (CnM) were manufactured by using MOSIS educational program with the ON-Semiconductor (0.35μm CMOS ICs manufacturing process). The main parameters of nMOSFETs can be found on the program's website educational MOSIS. The data sample was manufactured in the year 2015 and consists of 1 integrated circuit (IC). It was characterized 23 MOSFETs in this CMOS IC studied, with FnMs with different α angle (45˚, 90˚, and 135˚).

4. Device Matching Analysis

The figure of merit used to numerically qualify the device matching between the FnMs and their CnM counterparts is the relative error (ε_r) or also known as the variability coefficient, given in percentage, due to the CMOS ICs manufacturing process variations, is given by Equation (1) [9].

$$\varepsilon_r = \left(\frac{\left(\frac{s_{FnM}}{\bar{\mu}_{FnM}}\right) - \left(\frac{s_{CnM}}{\bar{\mu}_{CnM}}\right)}{\left(\frac{s_{FnM}}{\bar{\mu}_{FnM}}\right)} \right) \cdot 100 \qquad (1)$$

Regarding Equation (1), the s_{FnM}, s_{CnM}, $\bar{\mu}_{FnM}$ and $\bar{\mu}_{CnM}$ are respectively the standard deviations and the average values of a specific electrical parameter of the FnMs and their CnMs counterparts. The ε_r describes, in percentage, if the FnMs have a better (ε_r<0) or a worse (ε_r>0) devices matching in relation to their CnM counterparts. Thereby, the variability coefficient is used to measure the matching between devices for multiple different chips.

5. Experimental Results

For this sample of devices, the curves of the drain current as a function of the gate bias (i.e., the I_{DS} curve was generated as a function of V_{GS}), as well as the drain current as a function of the drain bias (ie, the curve of I_{DS} versus V_{DS}) of the FnMs and its equivalent CnMs, with the nMOSFETs operating in the triode and saturation regions, with the purpose of an analysis of the mismatch between devices, taking into account the following electrical parameters, which were extracted from the nMOSFETs of the V_{TH}(W/L) and I_{DSsat}/(W/L) considering different angles α (45˚, 90,0˚ and 145˚, respectively). The mismatch study between electrical parameters extracted from nMOSFETs FISH type and its conventional counterpart is performed through experimental comparative analysis between the relative errors behavior of the electrical parameters extracted from the FnMs and the CNMs counterparts, which is defined as the ratio between the standard deviation (s) and the mean value (μ) of the samples studied, that is, $s/\bar{\mu}$. Figure 2 illustrates the graph of relative errors between V_{TH}/(W/L) of the FnMs and its equivalent CnMs according to the angle α of the FnM, for a V_{DS} value of 50 mV (triode region).

Observing Figure 2, it can be seen that the FnMs with α-angles equal to 90˚ are able to produce a better matching between devices (-79.96%) when compared to those obtained from the CnMs. For the α angles equal to 45˚ and 135˚, it is also observed that the FnMs present a better matching between devices (-39.38% and -63.8, respectively) over the equivalent CnMs.Therefore, it is possible to conclude that the FISH-type nMOSFETs present a better matching between devices when compared to those observed by the CnMs, for all α angles studied. A justification for this behavior is due to the fact that the average values of the FnMs V_{TH}/(W/L) are higher than those observed in the CnMs regarding this range of α angles analyzed, due to, fundamentally, the presence of the Longitudinal Corner Effect (LCE), which is directly responsible for rising the resultant longitudinal electric field along the FISH nMOSFETs channel [7]. Figure 3 shows the graph of the relative errors between the I_{DSsat}/(W/L).

Analyzing Figure 3, it is observed that the relative errors of the I_{DSsat}/(W/L) presented a behavior similar to the observed in the analysis of the parameter V_{TH}/(W/L) concerning the devices FnMs and CnMs and therefore, conclude that FnMs devices have a better match between devices regarding the I_{DSsat}/(W/L) parameter when compared to the CnMs devices of -27.99% for angle α equal to 45˚, -85.01% for angle α equal to 90˚ and -76.03% for angle α equal to 135˚.

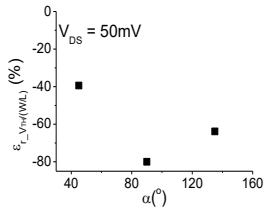

Fig.2 Graph of V_{TH}/ (W/L) as a function of the angle α of the FnMs, considering V_{DS} equal to 50 mV.

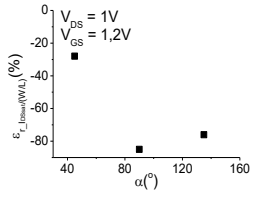

Fig.3 Graph of I_{DSsat}/ (W/L) as a function of the angle α of the FnMs, for V_{DS} equal to 1V and V_{GS} equal to 1,2V.

6. Conclusions

This study performed an experimental comparative study of the devices matching between the FnMs with different α angles and their CnM counterparts. The experimental results demonstrated that the FnM with α angles equal to 45˚, 90˚ and 145˚ are capable of boosting about 35%, in average, the devices matching in comparison to those observed with the CSnM counterparts, mainly because the LCE effects.

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Self-Recoverable Data Register Under Presence of SEE

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1. Abstract

The proposed data register design can keep the stored data valid after a single event effect (SEE) using integrity checking and a register clone. The data path uses tri-state buffers to accommodate a complex multiplexer and reduce the amount of silicon necessary for the implementation.

This data register structure could be expanded to build a register bank used in microprocessors improving the system reliability.

2. Introduction

High energy particles can strike sensitive nodes in digital circuits and cause upsets by changing memory and flip-flop contents or causing clock events in an unexpected moment[1]. A reliable circuit withstands such events with shielding or recovering from it. An usual solution for data registers with one or more bits would be Triple Modular Redundancy (TMR)[2] but it demands over 200% of resource usage and the majority voter is inherently difficult to design to reduce the sensitivity to SEE.

The proposed design, shown in Fig 1, duplicates the data register to both holds always the same content and provide means of recoverability. A parity bit is implemented as means of data integrity checking and is produced using a multiple input XOR gate. The three tri-state buffers, Z0, Z1 and Z2, form a multiplex circuit allowing the correct data content always present at Data Out with minimum resource usage. This approach of using tri-state buffers to form multiplexers has been used successfully in many designs[3]. When one bit of a data register is changed due to a SEE the fault is detected by the parity checking and will disable the tri-state buffer in use in order to kepp the correct data, from the other register, present at Data Out.

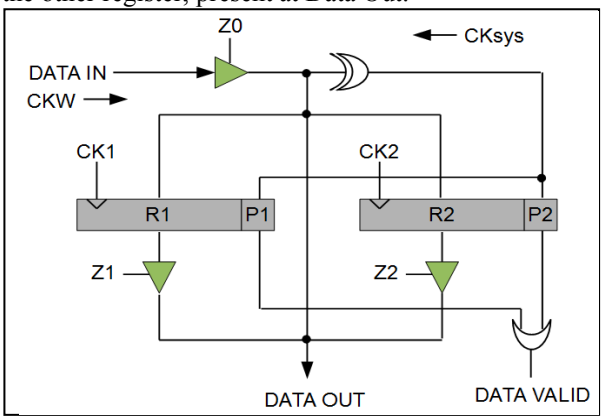

Fig.1. *Recoverable Data Register structure.*

Since the correct data at Data Out is also present at both register inputs a clock event can re-write the faulty register with correct data, recovering it from fault.

The write clock input (CKW) provides the timing for the circuit. A group of delay devices (not shown in the figure, as well as the logic gates for the circuit operation) are used to provide adequate sequencing for register's clocks and tri-state buffers.

For instance, when CKW is active the circuit must enable the tri-state buffer Z0 and disable the others. The registers' clocks (CK1 and CK2) must be delayed further due to propagation time of the parity evaluation circuit. Since a SEE can strike anywhere an added reliability can be obtained if CK2 is at least 1ns apart from CK1[4]. While Z0 is active due to CKW then Data Out will also presents the value. When CKW is released, the parity checking P1 of R1 shall drive the tri-state buffer Z1. CKW width must be enough to have both registers written and their parity bits checked before CKW is released. This would avoid some race condition and possible bus contention when Z1 and Z2 would be enable before R1 and R2 contents are the same. The logic governing the Z1 buffer is depicted in Fig 2. Z2 buffer has the same logic.

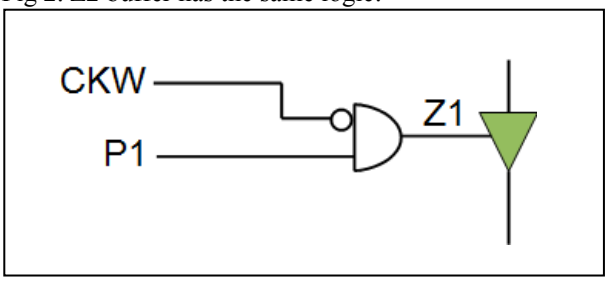

Fig.2. *Z1 Tri-State buffer logic.*

The logic will enable the Z1 buffer when CKW is not present and P1meaning the R1 data content is valid. The same will happen with Z2 and R2 and since both registers contains the same value they both can be active in the same bus with no harm to the system. In case R1 or R2 is changed due to a SEE the respective tri-state buffer will be disabled and the other register's buffer will remain active. There will be a momentary single bit race condition with opposite drive but it shall last for two logic gate delays, only, till the faulty register's buffer is disabled.

Another gate placed in the CK1 and CK2 clock inputs will allow a different external clock signal (CKsys) to re-write the faulty register. This clock can be generated by the system at any moment apart from

CKW but would be better if happening continuously and with short period to reduce the probability of another SEE striking the currently healthy register.

In the event of multiple upsets causing failures in both registers a Data Valid output would be deactivated, signalling other circuits that the Data Out bus content is invalid.

3. Timing

Fig 3 shows the timing diagram for this design. The first phase shows the circuit behavior when a new data is to be written. P1 and P2 may or may not be momentary inactive due to propagation delays. During this settling time the Data Out will contain the Z0 buffer's output while Z1 and Z2 are disabled.

When a fault is detected (red circle) and once CKW is inactive the CKsys clock is enabled to generate a new CK1 clock and re-write R1 with R2's contents. Since CKsys can cause a CK1 or CK2 clock only when CKW is inactive and P1 or P2 is also inactive this means CKsys can be a high frequency and cyclic clock signal.

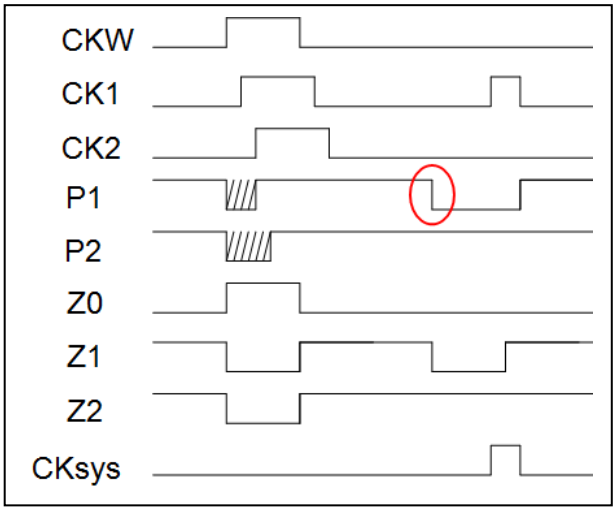

Fig.3. *Timing diagram.*

The delay mentioned before is seen with the displacement from CKW to CK1 and CK2.

Reliability under SEE is achieved by design. If a SET (Single Event Transient) in CK1 or CK2 happens in an unexpected moment it would only re-write the same contents in the registers. A SET in the CKW line would be absorbed by delay devices since a SET duration is known to be no longer than 1ns[4] and the delays can be elaborated to last a little longer. A parity error induced by SEU (Single Event Upset) would result in correct data and parity re-write and therefore be innocuous. A SET in one parity line, P1 or P2, would disable momentary one buffer but the other would keep the Data Out active with correct data.

The delay between CK1 and CK2 is also intended to absorb SET in the line between these signals[5], while providing sequencing and system's power reduction (less signals switching simultaneously).

4. Conclusions

The presented design shows a solution for data register reliability under SEE with few logic gates and simple register duplication. Parity checking is obtained with simple XOR gate with multiple inputs and delay devices can be constructed with cascaded inverters or other logic gates.

The design allows fast logic. Usually a data register write operation happens not as often as the system's clock cycle. The CKW to Data Out delay is equal of Z0 tri-state buffer delay, only, and all other timings are transparent to external system. Therefore, this design can be used in GHz systems without compromising the performance. The limitation is CKW width must be wider than the register and parity circuit delays.

Acknowledgments

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Optimization of a CMOS OTA Using an Interactive Genetic Algorithm

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1. Abstract

The designs of the analog CMOS integrated circuits (ICs) are complex due to the large number of design variables that must be determined to meet many desired specifications. Usually, they can be optimized by using heuristic algorithms of the artificial intelligence. This paper implements a novel approach using interactive (i) genetic algorithm (GA), iGA, to optimize analog CMOS ICs, including corner and Monte Carlo analyses in the loop of the optimization process. We optimized a single-ended single-stage OTA using the iGA focusing on changes of basic GA parameters during the optimization process, such as the weights of the desired specifications to assist the iGA convergence. The experiments performed with the iGA demonstrated to be capable of boosting the optimization cycle times in 63% in relation to the conventional GA.

2. Introduction

The designs of the analog CMOS integrated circuits (ICs) are complex and time consuming tasks due to the large number of design variables that must be determined to meet many desired specifications [1]. In this context, the multi-objective evolutionary algorithms (MOEAs) in the artificial intelligence area are appropriate and successfully used in the analog CMOS ICs optimization processes [2]. The MOEAs are classified into three categories [3]: 1) *a priori* category, which is used to generate solutions that try to achieve the best tradeoff among several pre-defined objectives according to the designer preferences; 2) *a posteriori* technique, which performs a wide search process to provide the designer with a set of solutions with distinct tradeoffs among the design specifications using the concept of Pareto optimality; 3) *progressive* category, which is based on the interaction of the designer with the optimization tool, in which the designer can progressively change design parameters, and specifications to assist the optimization process. The *progressive* category have been used in applications where subjective user evaluation is required, e.g. ergonomic chair design [4]. However, this technique have not been explored for the analog CMOS ICs optimization. This paper presents a novel approach to optimize analog CMOS ICs based on genetic algorithm (GA) incorporating the interactive (i) technique, iGA. The proposed iGA was integrated in the in-house optimization tool named MTGSPICE [5]. The aims of this work are to optimize an OTA using the proposed iGA approach and compare the effectiveness of the iGA with the conventional non-interactive GA.

3. Interactive Genetic Algorithm Methodology

Fig. 1 illustrates the flowchart of the iGA proposed in this work, integrated in the MTGSPICE [5], which uses the SPICE simulator and it performs robustness analyses (RAs) [corner analysis (CA) and Monte Carlo analysis (MCA)] in the loop of the optimization process [6].

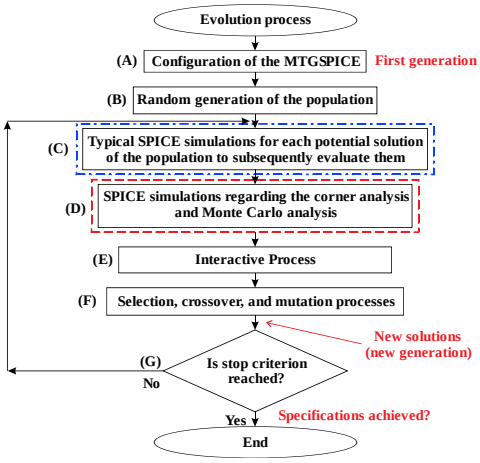

Fig.1. *Flowchart of the interactive genetic algorithm.*

Before starting the optimization the designer must configure the MTGSPICE (Block A), providing the circuit's description (SPICE *netlist*), input variables (transistors sizes and bias conditions), the desired specifications (FoMs) [open loop voltage gain, etc.], which are the output variables, with their respective tolerance ranges, and the GA parameters [population size (N_P), crossover and mutation rates (P_C and P_M), the weights (We_i) of each FoM of the fitness function [5], σ, which is the standard deviation of the Gaussian fitness functions [5], and N_{Rob} (the desired number of solutions contained in the population that fully meet the design specifications by the RAs), which is used as the stop criterion]. Next, the iGA generates randomly a set of N_P potential solutions (P) (Block B). Thereafter, in Block C, the potential solutions are simulated in SPICE (typical technology parameters) [6]. Next, in Block D, RAs are performed for feasible potential solutions found in order to evaluate their robustness (average error of the obtained FoMs) [6]. Then, the design variables, as well as the FoMs obtained by the most robust solution found in each generation of the optimization process are presented for the designer. Next, in Block E, the interactive procedure can be carried out. At this stage, the designer can pause the optimization process to change any parameter, such as P_C, P_M , We_i, and σ. Next, in Block F, the selection, crossover, and mutation genetic operators are applied to P to generate a new set of potential solutions for the next

generation [6]. The stop criterion is verified in Block G, which is obtained when N_{Rob} is reached.

4. CMOS OTA Topology

The OTA used in this work, illustrated in Fig. 2, is the single-ended single-stage (SESS) OTA [5].

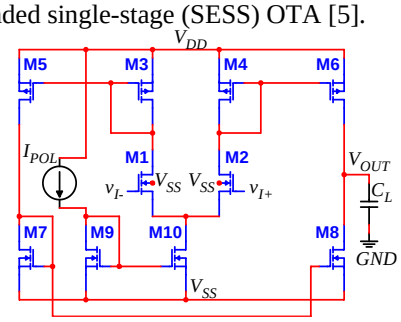

Fig.2. *Single-ended single-stage OTA architecture.*

5. Experimental Results

The desired FoMs (specifications) of the SESS OTA [5] are presented in Table I.

Table I. *Desired Design Specifications of the SESS OTA.*

Figures of merit (FoMs)	Specifications
Open loop voltage gain (A_{V0})	≥ 50 dB
Unit voltage gain frequency (f_T)	≥ 165 kHz
Phase margin (PM)	≥ 65°
DC output voltage (V_{OUT})	± 60 mV
Power consumption (P_{TOT})	≤ 5 µW
Gate area of the MOSFETs (A_G)	≤ 8636 µm^2

Regarding Table I, the tolerances of the specifications are adopted to be equal to ±10%. Moreover, all transistors are set to operate in the saturation region (functional constraints). The capacitive load (C_L) is adopted to be equal to 15 pF. Additionally, the supply voltages (V_{DD} and V_{SS}) are ± 1.5 V. The manufacturing process used to implement the OTA is the 350 nm from the ON Semiconductor. In addition, the ranges of values (minimum and maximum values) adopted for the optimization parameters, regarding the MOSFETs channel width (W) and length (L), and differential pair bias current (I_{POL}) for the SESS OTA optimization are 1-300 µm, 1-20 µm, and 0.01-1 µA, respectively [5].

Considering the initial values for the fitness functions parameters, the same weight (priority) is given for all desired design specifications: 16.7%, and σ is set to 0.2. The parameters related to the evolution process are set as follows: N_P=50; N_{Rob},=10 (number of robust solutions found by the optimization process by using RAs). In order to consider ten different sample results, the number of runs (N_R) regarding the optimization framework is equal to 10, in which each run uses a different seed for the random generator used by the iGA. At the end of these evolution processes, we have 10 N_{Rob} final potential solutions, where N_{Rob} solutions are obtained from each optimization run, which are selected from the population by the optimization process based on the corresponding smallest average errors regarding the FoMs obtained by each potential solution after the RAs. In the iGA implementation, P_C=0.7, and P_M=0.03. In addition the procedure adopted for the RAs are the same as those described in [6]. The interactive procedure used in the experiments focused on adjustments of We_i, and σ.

Table II presents the average values of the optimization cycle times (OCT) and the standard deviations (SD) in percentage regarding the average values of the ten optimization runs performed in the experiments using the conventional GA and the iGA.

Table II. *Optimization Cycle Times for the SESS OTA.*

Method	OCT (min.)	SD (%)
Non-Interactive	124.0	61.4
Interactive	45.7	23.3

Analyzing Table II, we observed that the iGA enabled a remarkable reduction in the OCT of the SESS OTA. In this case, the iGA reduced in approximately 63% the OCT required by the non-interactive approach. We observed also that the iGA presented a standard deviation 62% smaller than the non-interactive approach. Therefore, these results demonstrate that the iGA was remarkably more effective than the conventional GA and demonstrated a smaller dependence on the different GA initializations (initial populations). In addition, the potential solutions obtained by the iGA in the ten runs presented similar robustness to the conventional GA, that is, they presented similar average error regarding all FoMs of each potential solution with values around 5%.

4. Conclusions

This paper presented a new evolutionary approach to design analog CMOS ICs. The methodology is composed of an interactive genetic algorithm (iGA), which was integrated to the in-house optimization tool named MTGSPICE considering corner and Monte Carlo analyses in the loop of the optimization processes. Two experiments were carried out to optimize a single-ended single-stage OTA. In the first one, the conventional GA was used. In the second experiment, the proposed iGA was applied, where the designer interfered during the optimization process to change basic GA parameters. The experimental results demonstrated that the iGA is capable of reducing significantly the optimization cycle time and to obtain solutions robust to the environmental and manufacturing process variations.

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Study of OCTO type MOSFET (180nm Bulk CMOS technology of TSMC)

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1. Abstract

This paper compares a conventional gate geometry to a new gate geometry with an octagonal shape using a 180nm TSMC technology. The goal is to improve the electrical performance of the MOSFET, due to previous studies using different gate geometries, the results shown to be promising for this new geometry because of the new effects that appeared boosting the drain current and longitudinal electric field.

Keywords – OCTO, LCE, PAMDLE.

2. Introduction

With the development of integrated circuits (IC's), the research for new ways to improve the electric efficiency or to reduce the expended area of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has grown. There are many ways to improve the electrical performance, this paper uses a different layout of the gate.

Previous studies using different gate geometries confirm an existence of new effects. These effects were able to boost the drain current and the longitudinal electric field, causing an enhancement in the electrical performance of the MOSFET [1-2]. Provoking a will to study deeper these gate geometries, this paper will study an octagonal gate geometry using an 180nm technology of TSMC.

3. Device Characteristics

Fig. 1 exemplify the octagonal gate geometry.

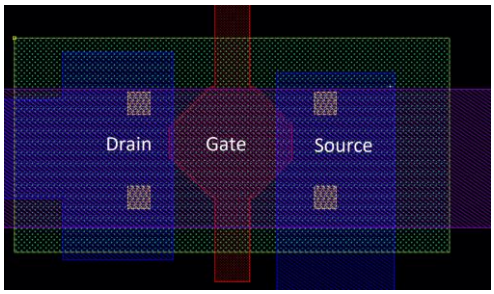

Fig.1. *Example of an octagonal gate geometry using the software "IC Station" of Mentor Graphics.*

This new geometry causes two new effects, the longitudinal corner effect (LCE), the parallel connections of MOSFETs with different channel lengths effect (PAMDLE) [1].

Due to the geometry, the longitudinal electric fields have different directions, causing an interaction between them, this interaction causes a sum of the longitudinal electric fields, therefore a bigger resultant longitudinal electric field and a bigger drain current, this effect is called longitudinal corner effect (LCE) [1]. The simulation presented in fig. 2 shows the interaction between the longitudinal electric fields, creating three areas of interaction, with one, two, or even three components of the longitudinal electric fields interacting [2].

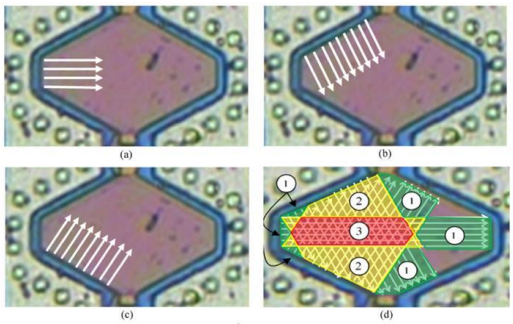

Fig.2. *Simulation showing the interaction between the longitudinal electric fields [2].*

Analyzing the gate by dividing it into 'n' parts along the width is possible to say that it is a parallel association of transistors and they have different channel lengths. Transistors with smaller channel lengths, located in the bottom and in the top of the gate, have a higher drain current, this effect is called PAMDLE, parallel connections of MOSFETs with different channel lengths effect.[1]

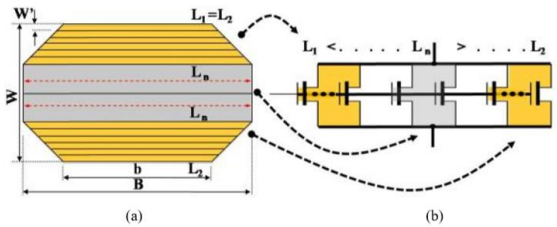

Fig.3. *Pamdle effect in an OCTO MOSFET, (a) an OCTO MOSFET with width divided in n parts and (b) equivalent circuit of the parallel association of the n transistors [2].*

Fig. 4 show the dimensions of the octagonal gate geometry, been, "B" bigger channel length, "b" smaller

channel length, “c” cut factor, “Li” one of the n transistors in a parallel association, “W” channel width and “α” angle of the geometry.

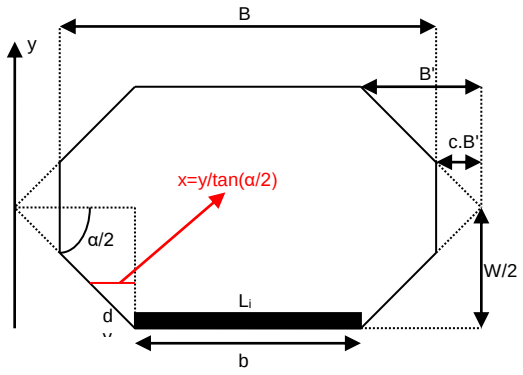

Fig.4. *Superior view of the octagonal gate geometry*

With a geometric analysis of fig. 4, we are able to obtain equation 1 that shows the equivalent channel length of a rectangular geometry with the same area of the octagonal geometry.

$$L_{eq} = b + \left[1 - \left(\frac{B-b}{2W}\right) tan\left(\frac{\propto}{2}\right)\right](B-b) \quad (1)$$

4. Experimental results

This section will present a comparison of the main electric parameters between a rectangular gate geometry and two octagonal gate geometry, with different cut factors “c” of 25% and 50%.

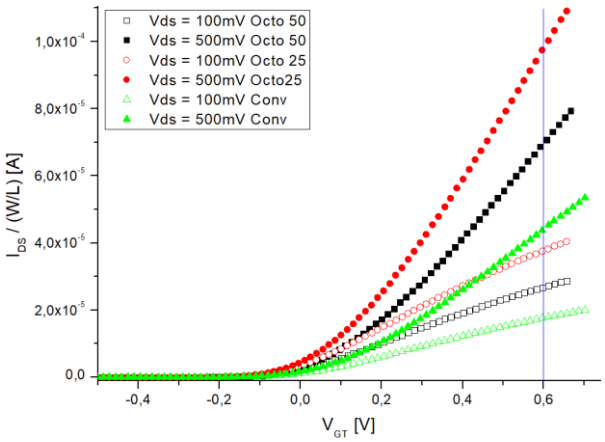

Fig.5. *Drain current divided by the geometry factor in function of the overdrive voltage.*

OCTO 25% was able to increase almost 100% and OCTO 50% almost 50% of the drain current compared to the rectangular gate geometry. Due to the LCE and PAMDLE effects combined to enhance the drain current. The fig. 6 show the drain current divided by the geometry factor in function of the drain voltage.

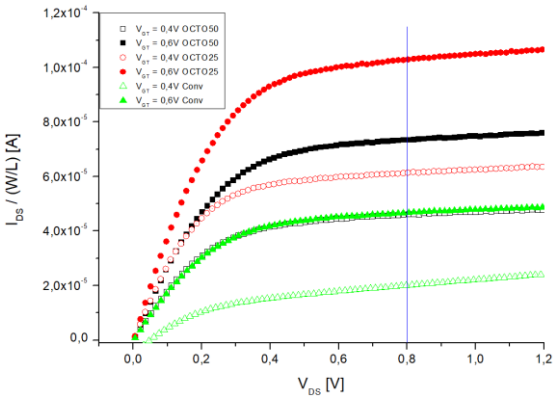

Fig.6. *Drain current divided by the geometry factor in function of the drain voltage.*

OCTO 25% was able to double the value and OCTO 50% increased more than 100% to an overdrive voltage (V_{GT}) of 0,4V, OCTO 25% increased more than 100% and OCTO 50% almost 50% to an V_{GT} = 0,6V of the drain current compared to the rectangular gate geometry. This increase in the drain current in function of the drain voltage reflects directly into the Early voltage (V_{EA}) increasing it and lowering the on-state resistance (R_{ON}), as shown in the table 1.

Table I. *Comparison of the geometries for on-state resistance and the Early voltage.*

Gate Geometry	On-State Resistance [Ω]		Early Voltage [V]	
	V_{GT} 0,4V	V_{GT} 0,6V	V_{GT} 0,4V	V_{GT} 0,6V
Conv.	12865	6449	-1,08	-6
OCTO25	4397	2968	-8,67	-10,6
OCTO50	6376	4176	-6	-9,67

4. Conclusions

This experiment prove the enhancement of the electrical parameters due to the LCE and PAMDLE effects in an 180nm TSMC technology. Boosting the drain current and the longitudinal electrical field, causing an enhancement of the Early voltage (V_{EA}) and a drop of the on-state resistance (R_{ON}), making this new gate geometry viable and opening a path to study more with different conditions and parameters.

Acknowledgments

We would like to acknowledge the Centro Universitário da FEI and the CITAR project, especially CTI Renato Archer with the support during the study and experiment of the MOSFETs.

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Comparative Study for g_m/I_{DS} of Ellipsoidal Layout MOSFET for 180 nm Technology

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1. Abstract

This article presents a comparative study for g_m/I_{DS} between the ellipsoidal and standard rectangular layout styles for Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), regarding the same bias conditions and the 180 nm CMOS ICs Manufacturing Process from TSMC.

The obtained results show that the electrical performance for the g_m/I_{DS} of the Ellipsoidal MOSFET is further improved when we compare with those observed regarding technological nodes led sophisticated due to the innovative effects (LCE and PAMDLE) that occur simultaneously in this innovative MOSFET structure.

2. Introduction

Currently high investments and many efforts are made to design ever smaller and better MOSFETs with analog and digital electrical characteristics [1]. There are many ways to try achieving these goals, among them we have the use of new materials for the fabrication of semiconductor devices, new planar and three-dimensional structures of MOSFETs and new manufacturing processes [1]. All these approaches require high investments or tend to increase the area of integrated circuits (ICs). Recently, an innovative layout technique has been proposed, using non-standard gate geometries or MOSFETs (hexagonal/diamond, octagonal/octo, ellipsoidal, waves and fish) [2-6]. This layout approach does not add any additional cost to the current manufacturing processes of the CMOS ICs. When we use these gate layouts to implement MOSFETs, new effects are incorporated into their structures: Longitudinal Corner Effect (LCE), Parallel Connection of Different MOSFETs with Different channel Lengths Effect (PAMDLE) and Deactivation of MOSFETs in the Bird's Beak Regions Effect (DEPAMBBRE) [3].

Several experimental studies on these innovative gate layout geometries for MOSFETs have shown that they are able to increase the electrical performance of MOSFETs compared to those observed when they are implemented with the rectangular layout style [5, 6]. A potential layout of gate for MOSFETs is the ellipsoidal gate geometry, which is the objective of this study (Fig. 1).

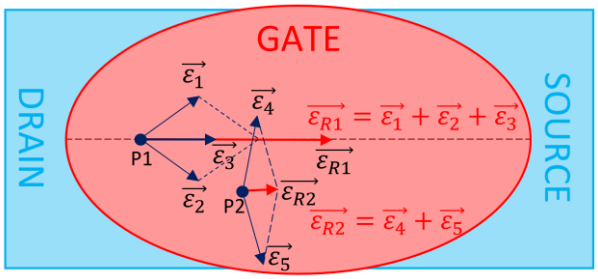

Fig.1. *The ellipsoidal MOSFET layout and the LCE.*

The MOSFET of the Ellipsoidal Gate (EGM) presents the LCE (represented in Fig. 1) and the effects PAMDLE and DEPAMBBRE [5]. The motivation of this work is to perform a comparative study of EGM and rectangular MOSFETs (RM), considering the same gate area (A_G) and bias conditions, in order to verify if the gains presented in the previous work (350 nm of ON-Semiconductor) about g_m/I_{DS} are preserved when we use a Complementary MOS (CMOS) integrated circuits manufacturing processes more sophisticated [5]. For analysis of the values obtained experimentally the data were normalized by the aspect ratio (W/L).

3. Ellipsoidal Gate MOSFET

Based on Fig. 1, we can see how the EGM gate region presents the LCE effect. In this region the longitudinal electric field is larger than that found in the RM counterpart. Consequently, the average velocity of the mobile carriers, which in turn the drain current (I_{DS}) along in the channel length of the EGM is higher than the ones observed in the RM counterpart. It is important to note that the more obtuse the ellipsoidal geometry, the greater the LCE effect in this structure.

4. Methodology

To compare the electrical parameters of these devices which present different gate geometries, its necessary to normalize their drain currents (I_{DS}) by their aspect ratios (W/L, where W and L are respectively the channel width and length). The EGM channel length (L_{EM}) which must be considered to normalize its I_{DS} correspond to a L of a RM that presents the same gate area that the one found in the EM, which is calculated by Equation (1) [5].

$$L = B.\pi/4 \quad (1)$$

Where B is the largest channel length along the ellipsoidal format gate.

The devices were manufactured with the 180 nm Bulk CMOS manufacturing process of the TSMC (implemented via mini@asic program of IMEC).

Table I presents the dimensional characteristics of the studied devices in this work.

Table I. *Dimensions of the devices considered in this work*

Device	Dimensions		
	W [µm]	L [µm]	W/L
Rectangular MOSFET (RM)	420	180	2.3
Ellipsoidal MOSFET (EGM)	1940	920	2.1

The devices were characterized by using the Keithley 4200-SCS and the threshold voltage (V_{TH}) of the EGM and RM obtained were 0.53 and 0.51 V, respectively.

5. Results

The Fig. 2 illustrate the g_m/I_{DS} curve as a function of $I_{DS}/(W/L)$ for V_{DS} equal to 400 mV.

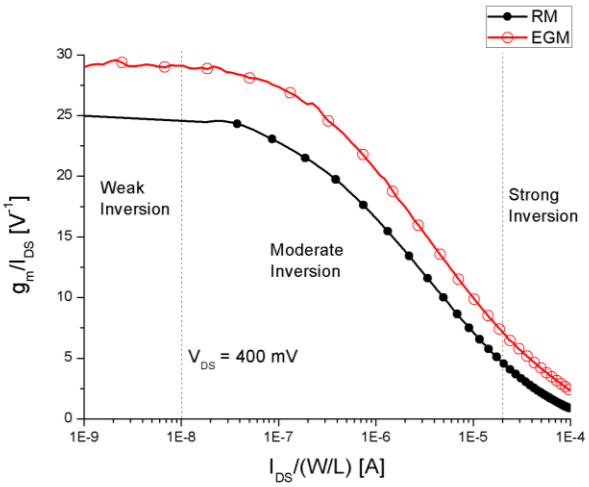

Fig.2. *The EGM and RM g_m/I_{DS} as a function of the $I_{DS}/(W/L)$ in logarithmic scale for V_{DS} equal to 400 mV.*

By analysing Fig. 2, it is notable that the EGM g_m/I_{DS} values are always higher in all inversion regimes (about 15 % in weak inversion, 24 % in moderate inversion and 105 % in strong inversion) than those measured in the RM equivalent, because the EM g_m values are much higher than those found in the conventional layout, due to the LCE and PAMDLE effects mentioned before.

6. Conclusions

A comparative study of the g_m/I_{DS} between the EGM and RM was performed, regarding the same bias conditions. Aiming to verify how the ellipsoidal layout even in more sophisticated technologies (180 nm of TSMC) remains a simple way to improve the electrical performance of MOSFETs. By exploiting the benefits of the LCE and PAMDLE effects commonly present in some unconventional gate geometries, it is possible to implement MOSFETs without requiring any additional cost for the current planar CMOS fabrication processes, only the layout change. With the gains of g_m/I_{DS} in all inversion ranges it proves to be a great choice for analog projects meeting requirements like efficiency and low cost.

Acknowledgments

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Proposal of a monitoring circuit for tandem solar cells

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1. Abstract

This work proposes a monitoring circuit capable of matching the short-circuit current density for the series configuration of tandem Si solar cells in order to increase the conversion efficiency besides the Shockley−Queisser limit of 29.8% [1,2]. The SPICE module of the Multisim 14 software was used for simulating the monitoring circuit composed of one Operational Amplifier (AmpOp) in a follower configuration to monitor two Si solar cells connected in the series tandem configuration. It was noteworth that the best conversion efficiency was obtained when the inverting and non-inverting inputs of the AmpOp short-circuited the output of one solar cell and followed the voltage drop of the second one. As a result, the conversion efficiency exceeded the mark of 30% using two starting solar cells in the series tandem configuration with individual efficiencies of 12% and 18%.

2. Introduction

During the last decade, the photovoltaic industry experienced stable market growth rates of between 15% and 20%, widely promoted by the energy market [1, 2]. The most efficient solar panels currently available in the industry have conversion efficiency up to 22.5%, while most of the panels available range from 14% to 18% [1,2]. It has recently been reported by the group of Surfaces and Interfaces of the LSI/PSI/EPUSP, MOS solar cells for Energy Harvesting applications with conversion yields of up to 12% with high degree of repeatability and reproducibility [1]. With the increase of research about conductive polymers, a new type of hybrid solar cell based on the joining of an inorganic semiconductor and a conductive polymer has become a reality and the cells have optical absorption and conductivity as an apparent advantage over the ease of deposition [3,4]. MOS solar cells have characteristics that leave them with high conversion efficiency, such as 16% (ITO/SiO_2/p-Si SIS) and 18.5% (MIS-IL) when compared to PN-junction Si solar cells[5-7].

The tandem structure consists of two Si solar cells conected in different configurations: series, module and four terminal [8]. This work shows a new approach to match the short-circuit current density for the series configuration of tandem Si solar cells in order to increase the conversion efficiency besides the Shockley−Queisser limit of 29.8%. To achieve this goal, the tandem structure was simulated with the help of the SPICE of the Multisim plataform in order to optimize their physical and electrical parameters. The starting point are conventional Si solar cells with different conversion efficiency to be connected in the series configurantion of the tandem structure.

3. Procedures and Results

The main parameters [1] of a Si solar cell are the Open- Circuit Voltage (V_{oc}), the Short-Circuit Current (I_{sc}) and the fill factor (FF). Figure 1 illustrates the relative current density I/I_{sc} and power $I.V/(I_{sc}.V_{oc})$ as a function of the relative voltage (V/V_{oc}). It is important to pay attention that Isc is the maximum current for V = 0 and Voc is the maximum voltage for I =0. The maximum in the power curve corresponds to the maximum value of the IxV product. The fill factor is defined as the relation between the maximum power and the product Isc.Voc as follows:

$$FF = \frac{V.I}{V_{OC}.I_{OC}} \quad (1)$$

The current through a silicon solar cell can be described by:

$$I_D = Ig - I_O.e^{\frac{V}{n.V_T}} \quad (2)$$

where Io is the dark current (without illumination) and Ig is the current generated in the Si solar cell. The conversion efficiency can be written as:

$$\eta = \frac{V_{OC}.J_{SC}.FF}{P_{in}} \quad (3)$$

where P_{in} is the incident light power on the area os the Si solar cell.

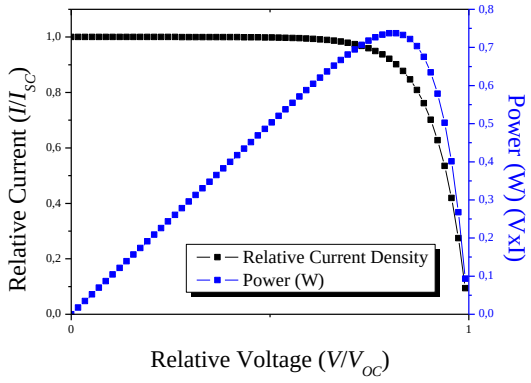

Fig.1. *Ilustration of the normalized J/Jsc x V/Voc*

Figure 2 illustrates the proposed monitoring circuit for the tandem Si Solar cell in the series configuration. It is composed of one Operational Amplifier (AmpOp) in a follower configuration to monitor two Si solar cells connected in the series tandem configuration. The first Si solar cell is represented by the model SC1 with I1, D1 R2 and R5 and the second solar cell of the series configuration is represented by the model SC2 with I2, D2 R3 and R4. R1 is the load resistance of the system formed by SC1, SC2 and the AmpOp. The inverting and non-inverting inputs of the AmpOp short-circuits the output of the SC1 and the voltage drop of the SC2 is followed by the output of the AmpOp. R4 and R5 are known as the series resistances and, R2 and R3 are known as the parallel resistances of the Si solar cells.

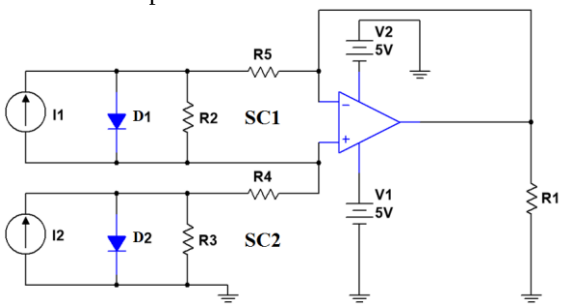

Fig.2. *Proposed monitoring circuit for the tandem Si Solar cell in the series configuration.*

Table I shows the simulating parameters of SC1 (MOS solar cell [1]) fabricated over a conventional PN solar cell SC2 [1]

Table I. *Especifications of the simulated SC1 and SC2 and the resulting parameters of the tandem Si solar cell.*

Par.	Tandem Si Solar Cell	
	SC1	SC2
I1, I2	20mA	40mA
R2, R3 (Ω)	100MΩ	100MΩ
R4, R5	12.5Ω	2Ω
FF	0.25	0.75
I_{SC}	20mA	40mA
V_{OC}	0.6V	0.6V
η	12%	18%
P_{in} (mW)	3mW	18mW
R1	12.2	
$I_{SC\ (tandem)}$	20mA	
$V_{OC\ (tandem)}$	2.4V	
η	32%	

Fig. 3 shows the resulting I x V characteristics of the tandem Si solar unit using a MOS solar cell (η = 12%) over a conventional solar cell (η = 18%) as simulated from the SPICE module of the Multisim platform. It is noteworthy that the resulting VOC of the tandem unit was three times higher compared to the individual values of the SC1 and SC2, respectively and the resulting conversion efficiency was 32%, which is higher than the Shockley−Queisser limit of 29.8%.

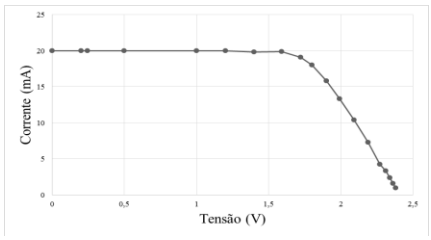

Fig.3. *Simulated IxV characteristic of the tandem Si solar unit using a MOS solar cell (η = 12%) over a conventional solar cell (η = 18%).*

An important operating condition is the load resistance close to the series resistance of the solar cell SC1, so that, the maximum power is transferred to the load and the solar cell operates at its point of maximum power (see equation 3).

4. Conclusions

A monitoring circuit capable of matching the short-circuit current density for the series configuration of tandem Si solar cells in order to increase the conversion efficiency besides the Shockley−Queisser limit of 29.8%. The best conversion efficiency was obtained when the inverting and non-inverting inputs of the AmpOp of the monitoring circuit short-circuited the output of one solar cell and followed the voltage drop of the second solar cell of the tandem unit. As a result, the conversion efficiency exceeded the mark of 30% using two starting solar cells in the series configuration with individual efficiencies of 12% and 18%.

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Test Facility for Electronic Devices Exposed to Ionizing Radiation

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1. Abstract

The study of the reliability of semiconductor devices exposed to ionizing radiation has intensified in recent years, mainly due to the ever-growing need to use more powerful and resourceful electronic devices in harsh environments as the space, nuclear medicine facilities, nuclear power plants or particle accelerators, in which radiation effects are important. However, with the automation of systems that are increasingly present also in the terrestrial environment, it is necessary to test electronic devices for the effects of radiation to be used, for example in autonomous vehicles, for greater reliability. This work presents the infrastructure of the Laboratory of Ionizing Radiation Effects (LERI: *Laboratório de Efeitos da Radiação Ionizante*), installed at the Centro Universitário FEI, whose mission is dedicated to testing and qualification of electronic devices -against Total Ionizing Dose (TID) effects.

2. Radiation Effects in Electronic Devices

The effects related to the incidence of ionizing radiation in electronic components have being studied more frequently by the scientific community, since its electronic devices may be submitted to adverse environmental conditions [1]. In the systems boarded in satellites and in aircrafts, which operate at high altitudes, electronic devices receive high radiation doses and are subject to the impact of charged particles which may affect its correct behavior [1]. The main effects of ionizing radiation and ion beams on semiconductor electronic devices are: TID (Total Ionizing Dose), SEE (Single Event Effect) and DD (Displacement Damage). Radiation effects affecting parameters in electronic components, causing degradation or functionality failure, have required special attention from Integrated Circuit (IC) designers and IC process engineers [2-4].

As an instance of a harsh environment, consider the Earth's high atmosphere, where charged particles (protons, electrons, and heavy ions) generated mostly by Sun's activity may be trapped in Earth's magnetosphere (the Van Allen belts), and high-energy photons (gamma and X-rays) are both present. At much lower altitudes, electronic systems embedded in airplanes are constantly targeted by neutrons [2]. The interaction of all these charged particles and photons with the atoms of the semiconductor devices generates a plethora of accumulative effects whose intensities are coarsely correlated with the absorbed dose of radiation in every electronic device, in some extent [5]. That's why it is always necessary to test the electronics that will be exposed to environments with ionizing radiation as to the radiation dose accumulated in the device.

The insertion of Brazil among the countries with aerospace technology and able to develop and launch satellites requires the development of electronic systems that are robust to the space environment, that is, systems that are capable of reliably gather, store, and process information for several years without maintenance. For these studies and to create experts in this strategic area in Brazil, facilities for Total Ionizing Dose (TID) and Single Event Effect (SEE) tests were created. In this work, several studies of damage mechanisms and methodologies of tests of electronic devices on tolerance to damage by exposure to ionizing radiation are presented. The test infrastructure at the Laboratory of Effects of Ionizing Radiation (LERI) installed at the Centro Universitário FEI will be presented.

3. Radiation test facility

A. Total Ionizing Dose (TID)

Total Ionizing Dose (TID) effects refer to the amount of energy absorbed by a unit mass of the material (dose). Particles with low Linear Energy Transfer (LET), that is, whose energy loss per unit length of its path through the medium is low, and electromagnetic radiation, tend to contribute more to this effect. TID effects can be generated when a photon interacts with the medium mainly by photoelectric effect, Compton effect or pair production. In any of these cases, electron-hole pairs are created in the material [1]. Since there is a sharp difference in mobility between electrons and holes in a typical oxide [1, 2], electric charge may become trapped in certain regions. This trapped charge may change the basic operating characteristics of the electronic device if it happens to sit near an electrically active region. Typical effects of TID on transistors, memories or FPGAs (transistor based devices) includes variation of the threshold voltage and of the subthreshold slope, leakage current induction, increase of the off-state current, and degradation of the on-to-off current ratio. Addionally,

since the presence or the absence of a charge packet in a specific cell is interpreted as the value for a particular bit, changes in electrical parameters have the potential to tamper with stored information [4,5].

Utilizing the facilities of the Centro Universitário FEI, we have conducted advanced research into the effects of X-ray radiation on electronic devices [3-5].

B. LERI - Laboratory of Ionizing Radiation Effect

Centro Universitário FEI's LERI is a laboratory dedicated to testing of the effects of ionizing radiation on electronic devices. The facility main irradiator is an X-Ray Diffractometer XRD-6100 Shimadzu with a 2.0 kW (maximum) Copper tube, that allows a beam current variation from 2 mA up to 50 mA, and an accelerating voltage variation from 20 kV up to 60 kV. The variation of these parameters allows the choice of different radiation dose rates up to hundreds of krad/s. With such a high dose rate it is possible to obtain high accumulated total dose in a short period of time. Using X-rays as radiation also facilitates the measurement of the electric parameters of the devices and circuits, such as the current as a function of the applied voltage in the DUT, as well as monitoring memories with respect to failures. All these electric measurements can be performed in real time during the irradiation test. This flexibility also allows the study of physical mechanisms, one of the goals in this project. Generally, a 10-keV X-ray beam is used, because in this case it becomes a convenient source of radiation due to its high performance in producing charges when compared to protons, alpha and heavy ions [3]. Another advantage of using X-rays to study TID is its accessibility compared with particle accelerators. In Figure 1 a general view of the laboratory is shown.

Figure 1: LERI general view.

The high charge density produced in the sensitive layers of the device occurs because the interaction of photons with the material is weaker than the interaction of ions with matter. Thus, when ions cross the oxide layer of a device, they generate, along their path, a dense column of electron-hole pairs that initially have a high probability of recombination. On the other hand, when X-ray photons interact with matter, electron-hole pairs are generated in a dispersed fashion, so that the average distance traveled by thermal diffusion by pairs is less than the average distance between pairs when they are generated. In this way, they have a lower recombination probability.

The X-ray equipment has already been properly studied and is suitable to perform experiments exposing electronic devices to ionizing radiation. In order to determine the effective average energy of the X-ray beam, the value of the semi-reducing layer was obtained through the attenuation curve for aluminum sheets of 99.9% purity, and the intensity of the radiation was measured through a 9015 Radcal monitor connected to an ionization chamber, aligned with the central axis of the beam. For a voltage of 20 kV applied in the Copper tube, an effective energy of approximately 10 keV was estimated. The absorbed dose values in electronic devices are estimated using appropriate mass attenuation coefficients for irradiated materials.

This laboratory was funded by Centro Universitário FEI and FINEP through the CITAR project.

4. Conclusions

The FEI radiation facilityallows research –in the physical mechanisms responsible for radiation damages in an electronic device or circuit. The results obtained in that research may support engineers in the task of designing to mitigate radiation damageand may also be used in device and circuit qualification processes for use in high radiation environments, such as the nuclear industries and space, which are strategic areas.

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