Using the Hexagonal Layout Style for MOSFETs to boost the Device Matching in Ionizing Radiation Environments

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Abstract— **This paper describes an experimental comparative study of the mismatching between the Diamond (hexagonal gate geometry) and Conventional (rectangular gate shape) n-channel Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs), which were manufactured in an 130 nm Silicon-Germanium Bulk Complementary MOS (CMOS) technology and exposed to different X-rays Total Ionizing Doses (TIDs). The results indicate that the Diamond layout style with an alpha (α) angle equal to 90° for MOSFETs is capable of reducing the device mismatching by at least 17% regarding the electrical parameters studied as compared to the Conventional MOSFET (CnM) counterparts. Therefore, the Diamond layout style can be considered an alternative hardness-by-design (HBD) layout strategy to boost the electrical performance and TID tolerance of MOSFETs.**

***Index Terms*— Diamond Layout Style, Hardness-by-design technique, MOSFETs matching, analog CMOS ICs, Total Ionizing Dose.**

I. INTRODUCTION

Considerable efforts and investments have been performed to improve the electrical performance, ionizing tolerance and devices' downscaling of Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) technologies, such as those related to new technologies, novel structures, innovative materials, new manufacturing processes, and novel device architectures and layout concepts [1-5]. Recently, some pioneering layout styles for MOSFETs were proposed which use the "Interface Engineering between the Drain/Source and Gate Regions", or simply "gate layout changing of MOSFETs" to boost the electrical performance and ionizing radiation tolerances of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). These innovative layout styles do not add any extra cost to current and sophisticated planar CMOS ICs manufacturing processes, such as the Bulk, Silicon-On-Insulator (SOI), Ultra-Thin Body SOI FETs (UTB) [6], Ultra-thin body and buried oxide (UTBB) [6-7], Double-Gate FET [7], etc. In this scenario, the Diamond (hexagonal gate geometry) layout style for MOSFETs is an example of this approach, according to Fig. 1, which illustrates an example of a layout of an n-channel Diamond SOI MOSFET (DnM) [8-9].

In Fig. 1, b and B are the smallest and largest channel lengths of the DnM, α is the angle between the pn metallurgical junctions composed of the drain/channel/source regions and W is the channel width. This innovative MOSFET structure is characterized by three new electrical effects. The first effect is called the Longitudinal Corner Effect (LCE). It is responsible for boosting the Resultant Longitudinal Electric Field (RLEF) and subsequently the drain current, transconductance, etc., compared to the Conventional (rectangular gate shape) MOSFETs (CM), n-type (CnM) counterparts, considering the same gate areas (A_G), Ws and bias conditions [8-9]. The second effect is called the Parallel Association of MOSFETs with Different Channel Length Effect (PAMDLE). As the DnM structure can be considered as the parallel connections of infinitesimal small conventional (rectangular) MOSFETs with different channel lengths (Ls) [indicated by the PAMDLE], each drain current (I_{DS}) tends to further flow by those infinitesimal MOSFETs that present the smallest channel lengths (Ls), which are found, initially, near the device edges. Therefore, the PAMDLE is responsible to decrease its effective channel length (L_{eff}) [Equation (1)] compared to the one of the CnM counterpart, in case that they have the same A_G and W, and consequently the drain current of DnM tends to be higher than the one of the CnM counterpart [8-9].

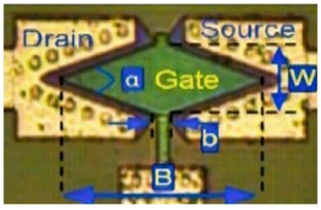

Fig. 1. Example of a DnM.

$$L_{eff} = \frac{B - b}{\ln\left(\frac{B}{b}\right)} \quad (1)$$

The third effect is called Deactivation of Parasitic MOSFETs in Bird´s Beak Regions Effect (DEPAMBBRE), because the RLEF lines in the Bird's Beaks Regions (BBRs) of the DnMs are curved, instead of straight and parallel lines, as happens for the CnM counterparts [8-9]. Consequently, the parasitic MOSFETs in the BBR of DnM are always electrically deactivated [8-9]. Thus, those three effects occur simultaneously in the DnM structure and they are responsible for boosting the DnMs electrical performance (LCE and PAMDLE) and Total Ionizing Dose (TID) tolerance (DEMPABBRE) in comparison to those found in the CnM counterparts [8-9].

Knowing that analog CMOS ICs are strongly influenced by the devices mismatch [10-13], the objective of this paper is to study the impact of the Diamond layout style for MOSFETs (n-type) on the devices mismatching, for devices

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that are not biased during the irradiation procedure (those spare parts or electronics that are not used during a space mission and posteriorly their functionalities are checked on the Earth for future uses).

II. Device Matching Analysis

The figure of merit used to quantify analytically the device mismatching of electrical parameters has adopted in this work is the coefficient of variation [$\varepsilon_{r(\%)}$] in percentage (%), due to CMOS ICs manufacturing process variations, which is given by Equation (2) [10-13]. Ideally, the electrical parameters must not vary with the increasing TID. Thus, the coefficient of variation expresses the measure of the dispersion of the manufacturing process and procedure of the X-rays ionizing radiations performed in order to estimate the variability of the devices [14-16].

$$\varepsilon_r(\%) = \left(\frac{\bar{\sigma}}{\bar{\mu}}\right).100 \quad (2)$$

In Equation (2), $\bar{\sigma}$ and $\bar{\mu}$ are the standard deviation and average value of the electrical parameter or figure of merit (FM) found in DnMs and their CnM counterparts.

III. Device Sample and X-ray ionizing radiation procedure

The DnMs and their CnM counterparts were manufactured by using a 130 nm Silicon-Germanium (SiGe) Bulk CMOS ICs technology. Fig. 2 illustrates the amount of chips used to develop this study and the results obtained of the coefficients of variation found after carrying out this study, which will be described along the text.

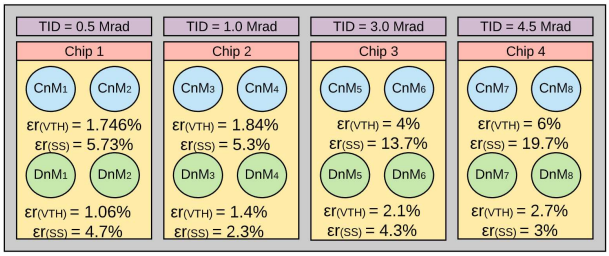

Fig. 2. Devices used to study the device matching.

According to Fig. 2, 2 DnMs and 2 CnMs were investigated for each chip ($Chip_{i=1, ..., 4}$). Therefore, the study has been performed with a total amount of 16 MOSFETs ($CnM_{j=1, ..., 8}$ and $DnM_{j=1, ..., 8}$). The values of the Ws and Ls of $CnM_{j=1, 3, 5, 7}$ are equal to 0.4 µm and 0.16 µm and of $CnM_{j=2, 4, 6, 8}$ equals to 0.8 µm and 0.16 µm, respectively. The values of W, b, B and alpha (α) angle for all DnMs ($DnM_{j=1, ..., 8}$) are equal to 0.56 µm, 0.20 µm, 0.88 µm, 90° (this technology node only allows to manufacture DnMs with the α angle equal to 90º), and the effective length of the DnMs is equal to 0.46 µm. Besides, each chip was exposed to a single dose, i.e., Chip 1: 0.5 Mrad, Chip 2: 1 Mrad, Chip 3: 3 Mrad and Chip 4: 4.5 Mrad. We have just used 4 chips (each one containing 2 DnMs and 2 CnMs) in order to take into account all potential possibilities of manufacturing process random variations and also of the procedure used to perform the X-rays ionizing radiations (local and global errors). Therefore, in order to improve the accurate of our study, we have decided to use the average and standard deviation values [17-19]. The distance between the chip and the exit of the X-ray beam is equal to 2.5 cm, the dose rate chosen to perform this study was defined by the value of (207 krad/h) and the average time between the end of X-ray irradiation and the beginning of electrical characterization is equal to 14 minutes, in order to guarantee that practically no annealing effect happened during laboratory experiments [20].

The devices were characterized by a Keithley semiconductor device analyzer, model 2636. The devices were irradiated with the Shimadzu X-ray diffractometer model XRD-6100 equipment at the CITAR laboratory at Centro Universitario da FEI, with a controlled temperature of 20°C and under open gate condition (floating gate). This work regards one of the possible studies that can be performed in order to analyzes the behavior of electronics or spare parts (replacement devices or redundancy devices) under the TID effects. Usually these devices are not biased during space missions and they are used only if any equipment presents some malfunction [21]. The electrical parameters were obtained from the drain current (I_{DS}) versus gate voltage (V_{GS}) curves, with a drain voltage (V_{DS}) of 50 mV to obtain the values of the threshold voltage (V_{TH}) and subthreshold slope (SS). Even though the channel width of the CnM are different from each other, both parameters studied on this paper mathematically do not depend on the channel width of the device. Therefore, even though the CnM devices have a slightly different channel width, the analysis of V_{TH} and SS could be done, so it is possible to develop this study. It is important to highlight that the Diamond MOSFETs present larger dimensions than those of the Conventional MOSFETs, and by the results obtained we can observe that the Diamond MOSFETs present a smaller variability than that of the Conventional MOSFETs. The authors consider that it would not be fair if the dimensions of the Conventional MOSFETs (gate areas: 0.06 µm^2 and 0.13 µm^2) were larger than those of the Diamond MOSFETs (gate area: 0.3 µm^2, at least 2 times higher) to perform this study, because we know that global random errors further affect the devices with larger dimensions.

IV. Experimental results and Discussion

Fig. 3 illustrates the pre-radiation and post-radiation coefficient of variation of V_{THs} of DnMs and CnMs counterparts, calculated by Equation (2), as a function of the TID. The coefficient of variation of V_{THs} and SSs in the zero-dose condition take into account all the 16 devices ($CnM_{j\ j=1, ..., 8}$ and $DnM_{j=1, ..., 8}$), while in post-irradiation conditions we only used 2 CnMs and 2 DnMs for each TID applied (Chip 1: $CnM_{j=1,2}$ and $DnM_{j=1,2}$; Chip 2: $CnM_{j=3,4}$ and $DnM_{j=3,4}$; Chip 3: $CnM_{j=5,6}$ and $DnM_{j=5,6}$; Chip 4: $CnM_{j=7,8}$ and $DnM_{j=7,8}$).

Regarding Fig. 3, for the initial condition, one observes that the coefficient of variation of threshold voltage (V_{TH}) for 8 DnMs and 8 CnMs are practically the same (difference of 3%). This occurs because the DnM's V_{TH} are approximately equal to 350 mV (typical value: 350 mV; maximum error: 10%) and standard deviations of these samples are practically the same too (approximately 1%). This is expected because these devices are implemented in the same CMOS ICs technology. However, as the TID increases, the differences

of the coefficient of variation (device mismatch) of DnMs and CnM counterparts increase. This happens because the coefficient of variation of the V_{THs} of DnMs are kept practically constant due to DEPAMBBRE that suppresses the parasitic MOSFET in the BBRs, while the coefficient of variation of CnMs increase [V_{TH} shifting to the left showing that there are more positive charges in the gate oxide (SiO_2) than at the SiO_2/Silicon (Si) interface] due to the X-ray ionizing radiation in the parasitic MOSFET in the BBRs of the CnMs, as the TID increases. Thus, DnMs present a higher X-ray TID tolerance at 1 Mrad than the one found in CnMs counterparts (DnMs: 2.0% and CnMs: 4.0% for a TID of 3 Mrad; DnMs: 2.7% and CnMs: 6.0% for a TID of 4.5 Mrad). Furthermore, the maximum difference between the V_{TH} coefficient of variation of the CnMs is 4.2%, while the one of DnMs is only 1.8%. This can be justified because the standard deviation of DnMs V_{TH} (3.5 mV) for a TID of 0.5 Mrad is the smallest value found in relation to others and the average value of DnMs V_{TH} is equal to 0.332 V, resulting in a coefficient of variation of 1.06%. For the pre-radiation condition, the standard deviation of DnMs V_{TH} is of 9.5 mV and the average value of DnMs V_{TH} is equal to 0.339 V, resulting in a coefficient of variation of 2.80%. Therefore, the difference between these two coefficients of variation results approximately in 1.8%.

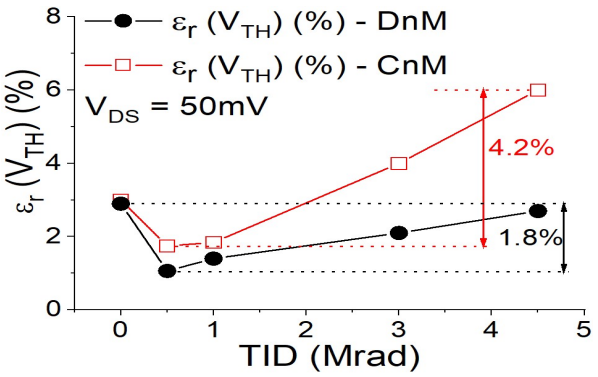

Fig. 3. The pre-radiation and post-irradiation coefficient of variation of V_{THs} of DnMs and CnMs as function of the TID for V_{DS}=50mV.

Based on Fig. 3, regarding V_{TH} coefficient of variation of devices, we can conclude that they present practically the same X-ray ionizing radiation tolerance (difference of 2.4%).

Additionally, Fig. 4 illustrates the pre-radiation and post-radiation coefficient of variation of DnMs SSs and CnMs counterparts, calculated by Equation (2), as a function of TID. The coefficient of variation of SSs in the zero-dose condition take into account all devices ($CnM_{j=1, \ldots, 8}$ and $DnM_{j=1, \ldots, 8}$), while in post-irradiation conditions we only used 2 CnMs and 2 DnMs for each TID applied (Chip 1: $CnM_{j=1,2}$ and $DnM_{j=1,2}$; Chip 2: $CnM_{j=3,4}$ and $DnM_{j=3,4}$; Chip 3: $CnM_{j=5,6}$ and $DnM_{j=5,6}$; Chip 4: $CnM_{j=7,8}$ and $DnM_{j=7,8}$).

Concerning Fig. 4, regarding the pre-radiation conditions, the SS coefficient of variation (device mismatching) of a sample of 8 DnMs is equal to 2.3%, while the SS coefficient of variation of the sample of 8 CnMs is 10.5%. This occurs because although the SS average value of DnMs (89.6 mV/dec.) is smaller than the SS average value of CnMs (95.9 mV/dec.), the standard deviations of the DnMs SS (2.1 mV/dec.) is smaller than that observed in the CnM counterparts (10.1 mV/dec.). This is mainly explained by the DEPAMBBRE, which bends the RLEF lines in the BBRs of DnMs, suppressing the parasitic MOSFETs placed in BBRs of the DnMs. Therefore, the positive charges induced at the interface of BBRs by the X-ray ionizing radiation do not influence the quality of part of the Silicon/Silicon-Oxide (Si/SiO_2) interface of DnMs, in contrast to what is happening at the Si/SiO_2 interface with the BBRs of the CnMs counterparts. Furthermore, as the TID increases, the differences between SS coefficient of variation of DnMs and CnMs increase significantly from 3 Mrad (9.4%: 4.3% for the DnMs and 13.7% for the CnMs) up to 4.5 Mrad (16.7%: 3% for the DnMs and 19.7% for the CnMs). This occurs because the SS coefficient of variation of the DnMs are kept practically constant due to the DEPAMBBRE, while the positive charges induced at the interface with the BBRs of CnMs by the X-rays ionizing radiation continue to increase when the TID increases. Besides, the maximum difference between the SS coefficient of variation (device mismatch) of CnMs is 14.4% (for 1 Mrad of TID: 5.3% and for 4.5 Mrad of TID: 19.7%) while for DnMs it equals 2.4% (for 1 Mrad of TID: 2.3% and for 4.5 Mrad of TID: 3%). These results show that the DnMs are more X-ray ionizing radiation tolerant than the one of CnM counterparts.

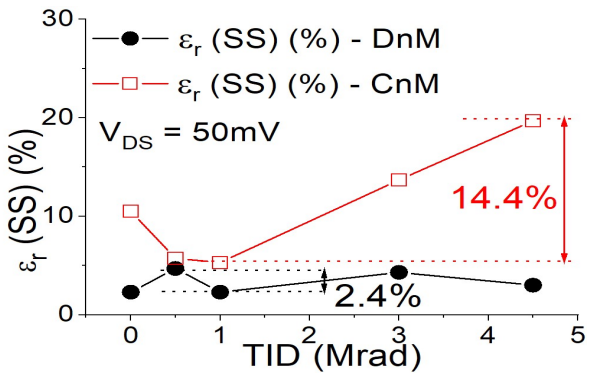

Fig. 4. The pre-radiation and post-irradiation coefficient of variation of SSs of DnMs and CnMs as function of the TID for V_{DS}=50mV.

Based on Fig. 3 and Fig. 4, one can also calculate three different FMs: I- the coefficient of variation of V_{TH} and SS of irradiated DnMs (2 samples for each TID) in relation to those observed for the irradiated CnMs (ε_{r1}) (2 samples for each TID). The calculation of the coefficient of variation ε_{r2} is regarding $V_{TH\ and}$ SS of irradiated DnMs (2 samples for each TID) in relation to their pre-radiated condition, of a total of 8 samples (Chip 1, Chip 2, Chip 3 and Chip 4). Additionally, the calculation of the coefficient of variation ε_{r3} is regarding the coefficient of variation of V_{TH} and SS of irradiated CnMs (2 samples for each TID) in relation to the pre-radiated CnMs of a total of 8 samples (Chip 1, Chip 2, Chip 3 and Chip 4). Table I summarizes the values found for ε_{r1}, ε_{r2} and ε_{r3}, respectively.

Based on Table I, the ε_{r1s} indicate that the coefficient of variation of the irradiated DnMs V_{TH} and SS are always smaller (V_{TH}: -40.7% on average; SS: -56.8% on average) than those measured for CnMs counterparts, thanks to the DEPAMBBRE present in DnMs. Therefore, DnMs present a

notably better device matching compared to CnM counterparts for all TIDs considered in this work. Thus, one can conclude that the Diamond layout style can be considered as an alternative Hardness-By-Design (HBD) technique to implement MOSFETs to remarkably boost the device matching, focusing on avionic, space and medical CMOS IC applications. Furthermore, the ε_{r2} indicates that the coefficient of variation (device mismatch) of the irradiated DnMs V_{TH} are always smaller than the coefficient of variation for the original devices and they reduce as the TID increases (-38.1% on average), i.e., the coefficient of variation ε_{r2} should be even closer to zero for a TID higher than 4.5 Mrad. Besides, for DnMs V_{TH}, we have verified that as the TID increases, the difference between the effects of the charges on the gate oxide (which causes the V_{TH} to be reduced) due to ionizing radiation is being compensated by the effects of the charges on the SiO_2 interface and the silicon film (which causes the V_{TH} to increase) and therefore there is a tendency for the V_{TH} to return to the pre-radiation condition. However, although the ε_{r3} of CnMs V_{TH} follows the same tendencies of DnMs V_{TH} up to 1 Mrad, they increase significantly beyond 1 Mrad, i.e., they do not tend to return to the pre-radiation values (+13.6% in average), as we have seen for DnMs. Moreover, the SS ε_{r2} calculated for DnMs, shows that the coefficient of variation of the irradiated DnMs are practically always higher than those of the starting devices [with a maximum variation of 2.4%, regarding Fig. 4] and they reduce as the TID increases, in contract to those observed for CnMs [with a maximum variation of 14.4%, regarding Fig. 4]. Therefore, DnMs present a better device matching, regarding V_{TH} and SS (maximum variation of 1.8% for the V_{TH} and 2.4% for the SS), after X-ray exposure compared to those of the pre-radiation conditions. However, the ε_{r3} indicates that V_{TH} and SS coefficient of variation of irradiated CnMs practically follow the same tendencies up to 1 Mrad and at this point they increase and do not tend to return to the pre-radiation condition (maximum variation of 4.2% for the V_{TH} and 14.4% for the SS), as we have seen for DnMs.

Table I. Values of ε_{r1}, ε_{r2} and ε_{r3} for the studied samples.

	(%)	Chip 1 TID = 0.5Mrad	Chip 2 TID = 1Mrad	Chip 3 TID = 3Mrad	Chip 4 TID = 4.5Mrad
V_{TH}	ε_{r1}	-39.1	-21.1	-47.4	-55.3
	ε_{r2}	-63.6	-50.5	-29.4	-8.8
	ε_{r3}	-41.2	-38.1	+32.3	+101.3
SS	ε_{r1}	-17.2	-57.1	-68.2	-84.8
	ε_{r2}	+102.8	-3.1	+86.1	+27.9
	ε_{r3}	-45.4	-49.6	+30.3	+88.3

Fig. 5 illustrates V_{TH} as a function of SS for the different TIDs applied to the DnMs and the CnM counterparts, for devices irradiated under gate floating conditions.

From Fig. 5, we can see that the behavior displayed on Fig. 3 and Fig. 4 can be justified by the changes on the average values and standard deviations of V_{TH} and SS of DnMs and CnMs, as the TID increases. Regarding V_{TH} of the devices, they decrease because a higher number of positive charges are induced in the gate oxide in comparison to those find in the interface composed by SiO_2 and the channel region. Concerning SSs of the devices, we can observe that they increase for both devices, as TID increases. This can be explained due to the higher number of the positive charges are induced by the X-ray ionizing radiations at the interface composed by SiO_2 and the channel region, as TID increases. However, we can see that DnMs were least affected, thanks to DEPAMBBRE present in their structures. Furthermore, on the pre-radiation condition, we observe that the standard deviation of DnMs V_{TH} is 27% smaller (9.5 mV) than the one of CnMs (13 mV), while they are practically the same for the different TIDs considered (maximum difference of 3.54 mV). Analogously, the standard deviation of the spreading of DnMs SS is 61.6% smaller (3.95 mV/dec.) in comparison to the one of CnMs SS (10.29 mV/dec.). However, the standard deviation of the spreading of DnMs SS do not change practically (maximum difference of 3.36 mV/dec.), while of the one of the CnMs increases (maximum difference of 22.28 mV/dec.), as the TID increases. The maximum differences for the CnMs V_{TH} and SS, regarding all TIDs, is equal to 0.1 V and 96.5 mV/dec., respectively, and the maximum differences for the DnMs V_{TH} and SS, for all TIDs, is equal to 0.09 V and 44.2 mV/dec. Thus, the experimental results indicate that DnMs present a higher X-ray TID tolerance than those measured in the CnM counterparts and therefore the Diamond layout style for MOSFETs can be considered an alternative hardness-by-design approach to improve the X-ray TID tolerance of MOSFETs.

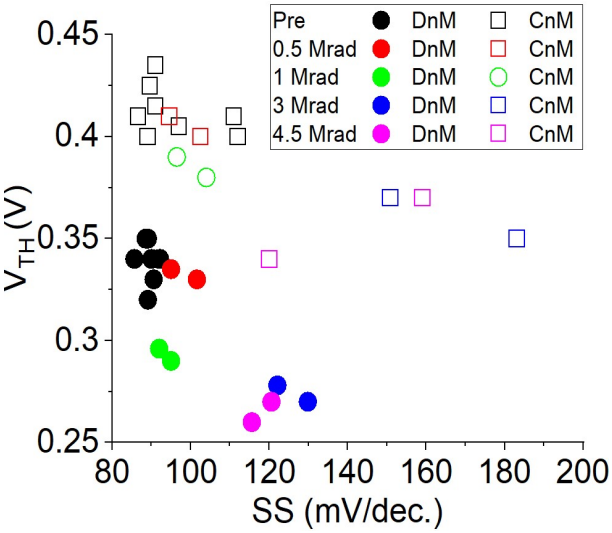

Fig. 5. V_{TH} as a function of SS for different TIDs analyzed.

V. Conclusion

This paper has performed an experimental comparative study of the mismatching between the DnMs and CnM counterparts under an X-rays ionizing radiation environment (maximum TID of 4.5 Mrad). The results show that the Diamond layout style (hexagonal gate shape) for MOSFETs with an α angle of 90˚ is capable of reducing the device mismatching (for V_{TH}: 21.1% and for SS: 17.2%) in comparison to those found in the CnM counterparts. This happens due the impact of the LCE, PAMDLE and mainly DEPAMBBRE present in the Diamond MOSFETs. Therefore, this layout approach can be considered an alternative Hardness-By-Design (HBD) technique to reduce the device mismatching of space and medical analog CMOS ICs.

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