Analysis of Mobility in Graded-Channel SOI Transistors Aiming at Circuit Simulation

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***Abstract*— This work presents an analysis of the behavior of the effective mobility of graded-channel FD SOI transistors using an Y-Function-based technique. Low field mobility, linear and quadratic attenuation factors were extracted from two-dimensional numerical simulations. The influence of the length of both channel regions over these parameters was analyzed. The parameters extracted from experimental data were used in a SPICE simulator, showing that it is possible to simulated GC SOI MOSFET using a regular SOI MOSFET model, by adjusting its parameters. This approach presents a percentage error smaller than 7.91% for low V_{DS}.**

Index Terms — Effective mobility, SOI, Graded-Channel transistors, Y-Function, SPICE simulation.

I. Introduction

Graded-Channel (GC) SOI MOSFET is an asymmetric channel transistor that has been proposed and demonstrated to improve SOI analog characteristics [1, 2]. Using a simple mask arrangement, the device channel presents two regions with different doping concentrations, a highly doped (HD) one near the source, with length L_{HD}, which is responsible for fixing the device overall threshold voltage (V_{th}), and a lightly doped (LD) one at the drain side, with length L_{LD} and reduced threshold voltage. Figure 1 presents a schematic representation of this device. By reducing the doping concentration near the drain, the electric field is substantially diminished, reducing the impact ionization. It has been shown that fully depleted (FD) SOI GC nMOSFETs provides larger transconductance (g_m) and reduced output conductance (g_D), being very attractive for analog applications [3, 4].

Analytical models that describe electrical characteristics of the devices are necessary to allow simulations required for the design of analog circuits. An analytical model has been proposed for GC SOI MOSFET [5] and considers the asymmetric channel transistor as a shorter one, given by HD region, whose drain voltage is modulated by LD region.

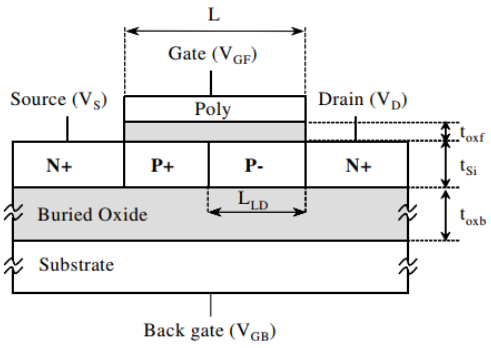

Fig.1 Cross-section of a GC SOI nMOSFET.

Although it has shown good agreement with experimental measurements, this model is not available in commercial circuit simulators. However, several models for SOI transistors can be found in simulators libraries.

In this work, the effective mobility of GC SOI nMOSFETs is analyzed. The low-field carrier mobility and two mobility degradation coefficients are extracted and used as adjusting parameters in order to adapt available SOI MOSFET models to simulate this asymmetric channel transistor.

II. Numerical Simulations

In order to study the behavior of the effective mobility of GC FD SOI nMOSFETs, Sentaurus TCAD simulations were performed [6]. All simulated devices present silicon film thickness t_{Si} = 80 nm, gate oxide thickness t_{oxf} = 31 nm, buried oxide thickness t_{oxb}= 390 nm, highly doped region doping $N_{A,HD}=5.6\times10^{16}$ cm^{-3} and lightly doped region doping $N_{A,LD}=10^{15}$ cm^{-3} [7]. Transistors with channel width (W) of 1 µm and different channel lengths (L) and L_{LD}/L ratios were simulated, using model parameters adjusted to experimental data as in [8, 9].

The simulated curves of drain current (I_{DS}) and transconductance (g_m) as function of gate-to-source voltage drop (V_{GS}) are exhibited in Figure 2, for different GC SOI transistors with L=2 µm, at drain voltage (V_{DS}) of 50 mV. It can be observed a raise of drain current level and transconductance with L_{LD}/L ratio increase. In accordance with the literature, the maximum transconductance of GC SOI MOSFETs increases with L_{LD}/L increase [1, 2, 5]. However, for larger gate voltages, g_m curves become close to that of a uniformly doped transistor with the same total length (L). This characteristic is usually attributed to the dependence of effective

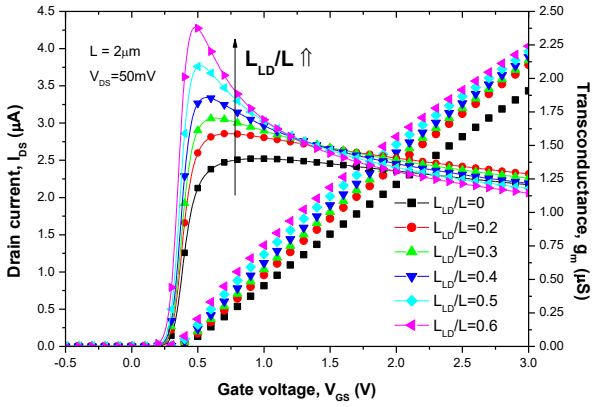

Fig. 2 Simulated curves of I_{DS} vs. V_{GS} and g_m vs. V_{GS} for GCSOI nMOSFETs with L= 2 µm and V_{DS}=50 mV.

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channel length on applied voltages presented by GC transistors. For V_{GS} below V_{th}, LD region is already in strong inversion regime and the GC transistor acts as a shorter device (with effective channel length L_{eff} close to L_{HD}). In this situation, there is a large difference between the electron concentration in the inversion layer at the HD and LD regions. However, as V_{GS} becomes larger than V_{th}, the electron concentration in the surface of both GC SOI channel regions becomes similar, and the effective channel length of the transistor tends to L as shown in [10], reducing g_m, but still with larger current. As can be seen in Figure 2, the increase of L_{LD}/L ratio results in larger I_{DS}, due to L_{eff} decrease.

Another way to understand this behavior would be to consider the transistors channel length fixed and equal to its total mask length ($L=L_{HD}+L_{LD}$), but with low-field mobility and degradation increasing with L_{LD}/L. Therefore, with the aim of analyzing the effective mobility of GC SOI with different channel lengths and lightly doped region channel lengths, the Y-Function method [11] has been used to obtain the low-field mobility (μ_0), and the linear and quadratic attenuation factors θ_1 and θ_2, respectively. Then, the effective mobility (μ_{eff}) is modeled by eq. (1) [11, 12], where $V_{GT} = V_{GS} - V_{th}$.

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1 V_{GT}+\theta_2 V_{GT}^2} \quad (1)$$

According to [13], θ_1 accounts for phonon and Coulomb scattering mechanisms, while θ_2 would consider surface roughness of the channel-silicon oxide interface. However, not only the effects of mobility scattering mechanisms are comprised in the attenuation factors, since the series resistance is also included in θ_1 [11, 12].

Figure 3 presents the low-field mobility as a function of L_{LD}/L ratio extracted from I_{DS} vs V_{GS} curves simulated at V_{DS} = 50 mV, of GC transistors with total length of 1 µm, 2 µm and 4 µm. Note that $L_{LD}/L = 0$ represents a conventional uniformly doped transistor. As presented in these results, low field mobility increases with L_{LD}/L. These results could be associated to a lower phonon and impurity scattering in the lightly doped region compared to the highly doped one. Therefore, as LD region presents larger mobility, the increase of its length with the L_{LD}/L ratio contributes to the increase of the overall mobility of GC transistor. Also, one can note a small variation of the mobility with respect to the channel length. This might indicate that for a given technology, GC mobility depends on the relation between HD and

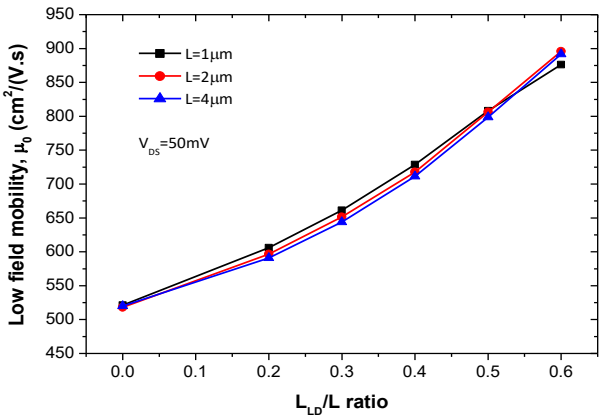

Fig. 3 Extracted low field mobility as a function of L_{LD}/L ratio for different total channel lengths.

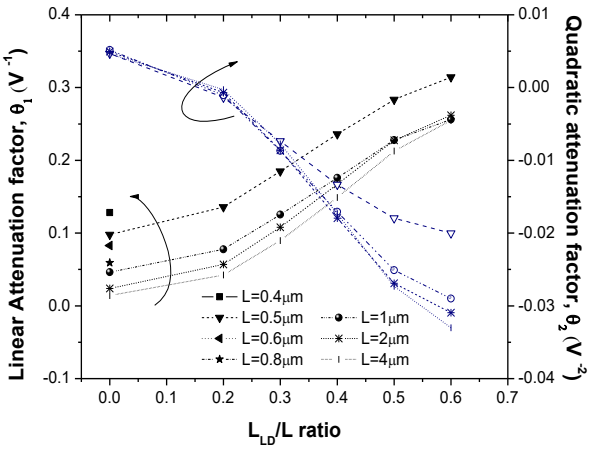

Fig. 4 Extracted linear and quadratic attenuation factors as a function of L_{LD}/L ratio for GC transistors with different total channel lengths.

LD lengths and not on the total L.

Extracted linear and quadratic attenuation factors are presented in Figure 4 as a function of L_{LD}/L ratio for L ranging from 0.4 µm to 4 µm. As one can see while the linear attenuation factor θ_1 increases with L_{LD}/L, the quadratic attenuation factor θ_2 decreases, even becoming negative with the raise of L_{LD}/L ratio. In addition, θ_1 and θ_2 are dependent of the total channel length L. As L decreases for the same L_{LD}/L ratio, θ_1 becomes higher and θ_2 get closer to zero, so that for short channel lengths the degradation on transconductance is high. Whereas for long channel lengths, the more negative θ_2 cancels part of the θ_1 effects what makes the degradation in this case, lower.

Observing the transconductance curves and considering the direct relation between g_m and μ_{eff}, it is possible to see that the mobility degradation increases as L_{LD}/L ratio increases, specially right after g_m peak. In this region, with low V_{GT}, the predominant degradation coefficient is θ_1. Its increase might be related to the series resistance. The increase of L_{LD} length would contribute to increase the resistance, making the linear attenuation factor θ_1 larger. For uniformly doped transistor, an increase of θ_1 is observed for short-channel devices, whereas it is less dependent on L for longer transistors, as in Figure 4. For GC transistors, θ_1 increases with L_{HD} decrease (L_{LD}/L increase). However, comparing a GC and a uniformly doped transistor with $L = L_{HD}$, larger θ_1 is seen for the GC device, indicating that not only the HD region impacts the effective mobility of the overall structure. Then, the GC MOSFET could be understood as a shorter transistor given by HD region.

On the other hand, the increase of LD region length has shown to promote the reduction of θ_2, that has resulted in negative values for $L_{LD}/L > 0.2$. Even though a negative mobility degradation factor might sound unphysical, theoretical works predicted that θ_2 may be negative [12] for transistors with low doping levels. In this case, the negative θ_2 acts to compensate the increase of θ_1. In fact, as can be seen from the g_m vs V_{GS} curves, as gate voltage is increased, mobility degradation is attenuated, and this attenuation is larger as L_{LD}/L is raised. It has been observed that it is not possible to reproduce I-V curves with the simple mobility model, where $\theta_2 = 0$.

The reduction of of mobility degradation in GC SOI transistors is related to the smaller electric field in comparison to

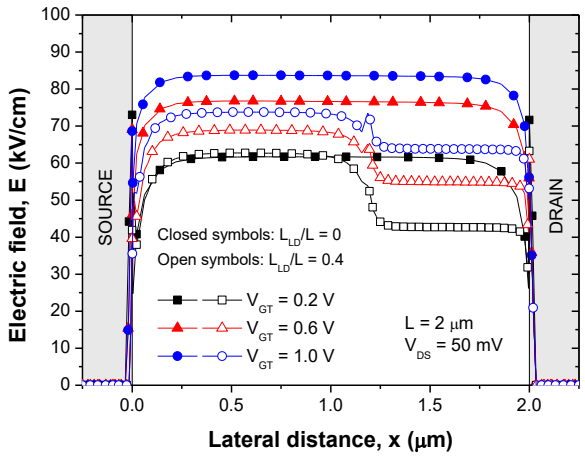

Fig. 5 Electric field along the channel length, extracted from numerical simulations of curves of GC SOI with L = 2μm, L_{LD}/L = 0 and 0.4 at different V_{GT} and V_{DS} = 50 mV.

uniformly doped one. The reduction of electric field can be seen in Figure 5, that presents the electric field as a function of lateral distance extracted from the simulations, for uniformly doped and a GC SOI with L_{LD}/L = 0.4, both with L = 2 μm, at 5 nm below the gate oxide at different V_{GT} values. The reduction of electric field has shown to increase with L_{LD}/L, and results in smaller mobility degradation in GC transistor in comparison to the uniformly doped one with same total length.

The results presented so far were obtained for fixed L, and

Table 1 – Dimensions of simulated GC SOI transistors and extracted threshold voltage.

L_{HD} [μm]	L_{LD} [μm]	L [μm]	L_{LD} / L	V_{th} [mV]
0.50	0.25	0.75	0.33	318
	0.50	1.00	0.50	298
	0.75	1.25	0.60	284
	1.00	1.50	0.67	269
	1.25	1.75	0.71	278
	1.50	2.00	0.75	271
0.25	0.50	0.75	0.67	170
0.50		1.00	0.50	298
0.75		1.25	0.40	339
1.00		1.50	0.33	356
1.25		1.75	0.28	367
1.50		2.00	0.25	374

then L_{HD} and L_{LD} were varied at the same time. To explore the influence of HD and LD region lengths on the low-field mobility and its degradation factor, simulations were performed with fixed L_{HD} and different L_{LD}, and with fixed L_{LD} and different L_{HD}. Figures 6 and 7 exhibits the transconductance as function of gate voltage for GC transistors with L_{HD} = 0.5 μm and L_{LD} = 0.5 μm, respectively. In both cases, the other channel region has been varied from 250 nm to 1.5 μm, resulting in total length ranging from 0.75 μm to 2 μm. Table I presents the simulated length and resulting L_{LD}/L, as well as the V_{th} extracted using Y-function. As expected, when HD region has been fixed, V_{th} is barely affected by LD region change. A small reduction (less than 50 mV) is observed when increasing L_{LD} from 0.25 to 1.5 μm, due to the increase

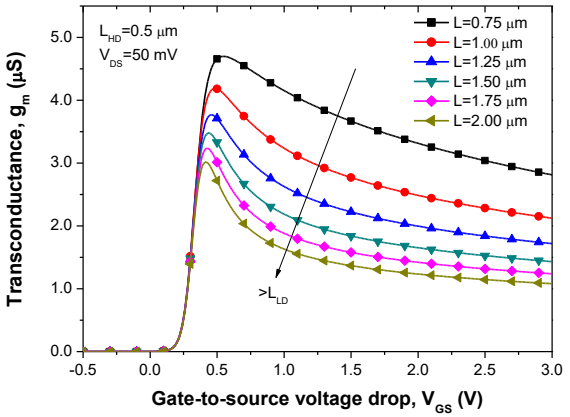

Fig. 6 Simulated curves of g_m vs. V_{GS} for GC SOI transistors with fixed L_{HD} = 0.5μm and different total channel lengths, V_{DS} = 50 mV.

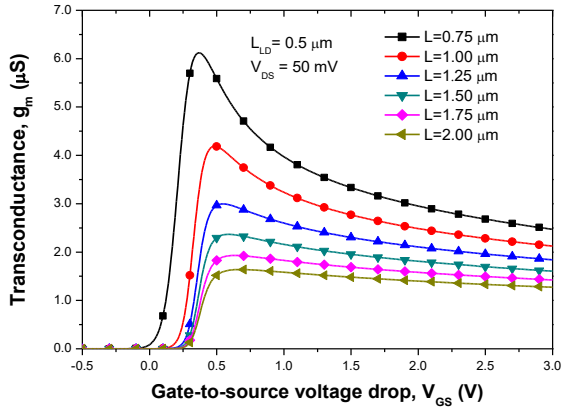

Fig. 7 Simulated curves of g_m vs. V_{GS} for GC SOI transistors with fixed L_{LD} = 0.5μm and different total channel lengths, V_{DS} = 50 mV.

of resistance. However, L_{HD} reduction led to the occurrence of short-channel effect, reducing V_{th}, also seen through the displacement of g_m curves in Figure 6. By observing the curves presented in Figure 6 and 7, one can note that the increase of L_{LD} causes larger mobility degradation than the increase of L_{HD}.

The extracted values of μ_0 mobility are presented in Figure 8 as function of HD and LD region lengths for fixed L_{LD} and L_{HD} respectively. The mobility increases as L_{LD} becomes longer for fixed L_{HD}. It is related to the larger mobility observed when doping concentration is reduced. Therefore, by having most of the total channel length lightly doped, the resulting μ_0 increases (black squares). On the contrary, when L_{LD} is fixed and L_{HD} is increased (red stars), a reduction of μ_0 is observed, which agrees with the hypothesis that the overall μ_0 results from the combination of μ_0 of both regions, and weighted by their lengths. Similar approach has been obtained in [14]. The influence of L_{LD} increases is more pronounced than L_{HD} increase. While μ_0 has increased more than 70% when L_{LD} increased from 0.25 to 1.5 μm, the reduction due to L_{HD} increase was about 30%.

Figure 9 presents the mobility attenuation factors, θ_1 and θ_2 as a function of L_{LD} (A) and L_{HD} (B). It can be seen that as the overall μ_0 increases, θ_1 also increases, both with L_{LD} increase or L_{HD} reduction. As θ_1 increases, θ_2 becomes negative and with higher absolute value, in order to attenuate the high degradation observed at high V_{GT}. As for the mobility, the LD region length seems to have higher influence on the overall effective mobility of GC transistors.

III. Experimental Measurements and SPICE Simulation Validation

Graded-Channel SOI nMOSFETs were fabricated using FD SOI technology from UCLouvain, featuring the same technological parameters used in the simulations [7], channel width (W) of 20 µm, and channel length L = 1 µm and 2 µm, and different L_{LD}/L ratios. The effective L_{LD}/L ratios were extracted as shown in [1, 2].

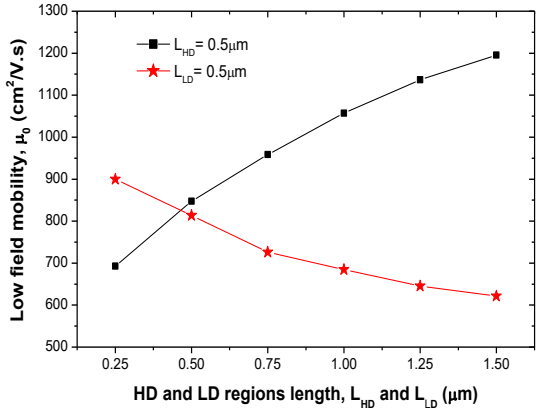

Fig. 8 Low field mobility as a function of L_{LD} and L_{HD} channel length for fixed L_{HD}= 0.5µm and L_{LD}= 0.5µm.

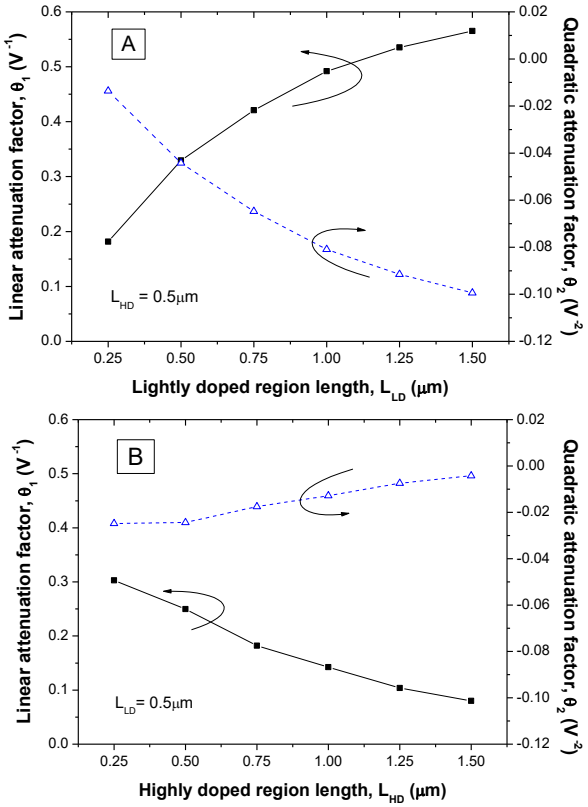

Fig. 9 Linear and quadratic attenuation factors (θ_1 and θ_2) as a function of L_{LD} for a fixed L_{HD}= 0.5µm (A) and as a function of L_{HD} for a fixed L_{LD}= 0.5µm (B) .

Figure 10 presents the extracted low-field mobility as a function of L_{LD}/L ratio. As predicted from simulations, both the increase of L_{LD} and decrease L_{HD} contribute to increase μ_0. Also, even changing the total length, μ_0 is slighted affected.

The mobility attenuation factors are presented in Figure 11 for L = 1 µm (A) and L = 2 µm (B), showing the same tendency of numerical simulations.

Aiming at validating the proposal of simulating GC SOI MOSFETs using a regular SOI model with adjusted parameters, the extracted values of low-field mobility and attenuation factors were used to obtain I_{DS} vs V_{GS} curves with a SPICE simulator. Simulator ICAP4 [15] has been used and simulations were performed with BSIM SOI v3.2 model [16], which uses linear and quadratic mobility attenuation factors to obtain the effective mobility.

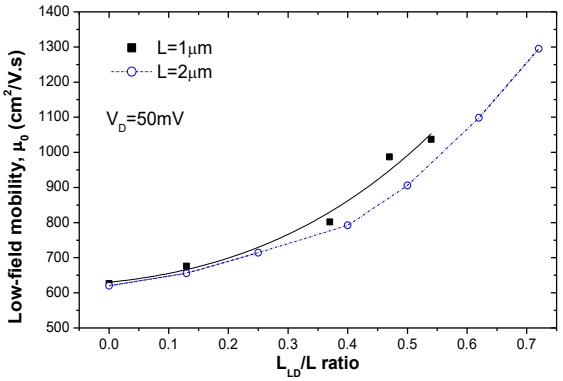

Fig. 10 Low field mobility as a function of L_{LD}/L extracted from experimental measurements of GC SOI transistors with L= 1 µm and L= 2 µm.

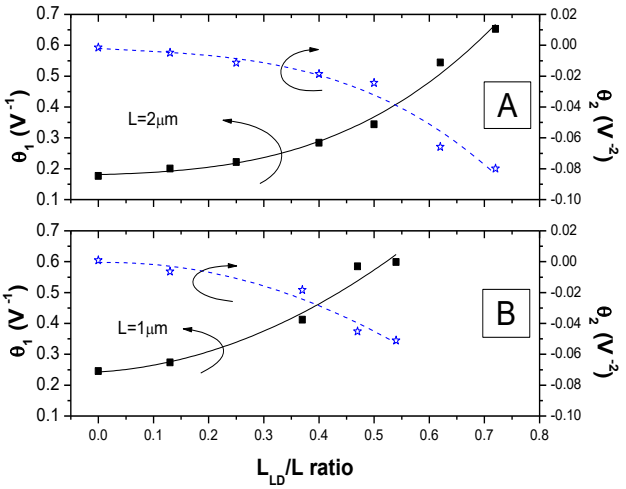

Fig. 11 Linear and quadratic attenuation factors as a function of L_{LD}/L ratio extracted from experimental measurements of graded-channel transistors with L= 2µm (A) and L= 1µm (B).

Figure 12 presents the comparison of experimental data and SPICE simulations of I_{DS} and g_m curves as a function of V_{GS} for GC SOI nMOSFET with L = 1 and 2 µm and different L_{LD}/L ratios, with V_{DS} = 50 mV. The obtained results show that the simulated curves have a good agreement with experimental results for both L values.

However, as most analog circuits operate in saturation, at higher V_{DS} values, simulations were also performed for the GC SOI nMOSFETs with L = 2 µm at V_{DS} = 1.5 V. The results are presented in Figure 13 and has shown a good fitting in saturation region, that is the region of interest. It is worth mentioning that apart from technological and geometrical characteristics, only the following parameters were adjusted: μ_0, θ_1 and θ_2.

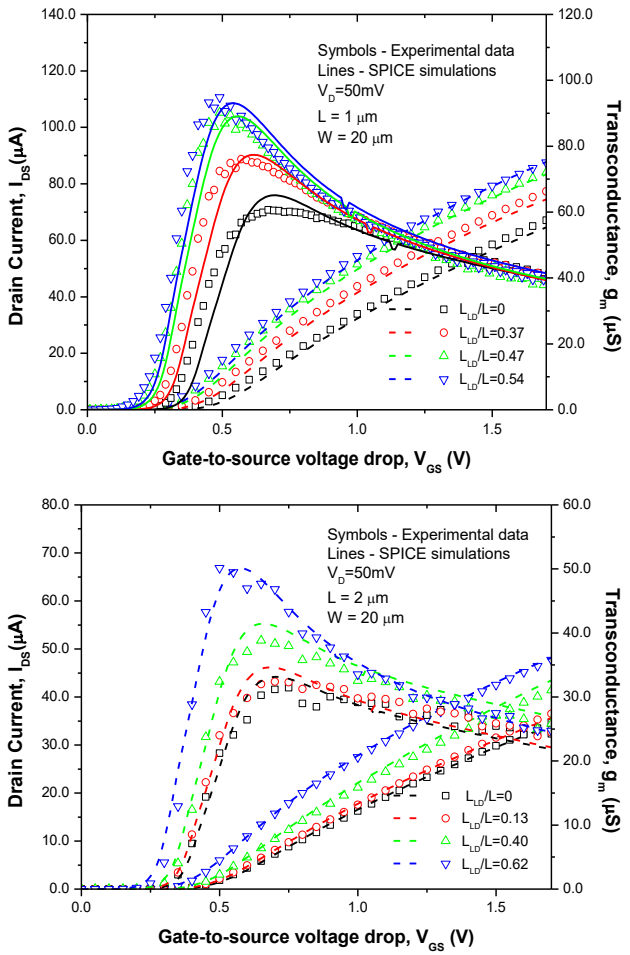

Fig.12 – Comparison of drain current and transconductance curves obtained through analytical simulations and experimental measurements for GC SOI nMOSFETs with L= 1 and 2 μm, at V_{DS} = 50 mV.

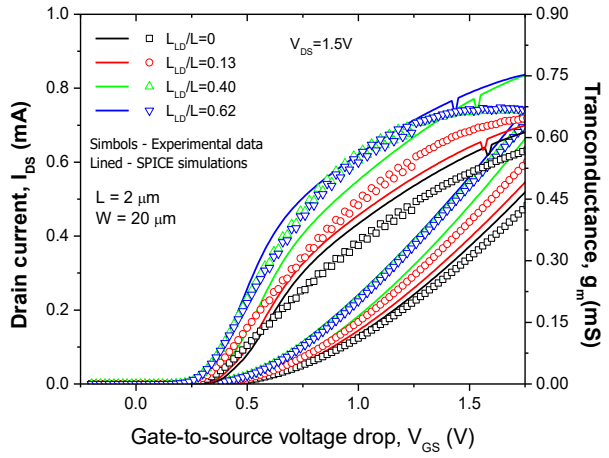

Fig.13 – Comparison between SPICE simulations and experimental drain current and transconductance curves obtained or GC SOI nMOSFETs with L= 2 μm, at V_{DS} = 1.5 V.

IV. Conclusions

In this paper, the mobility of graded-channel SOI transistors was investigated. By using two-dimensional numerical simulations, drain current curves of transistors with different total channel length and L_{LD}/L ratios were obtained. It has been observed that the simple mobility degradation model, with only linear attenuation factor is not capable of describing GC SOI I-V curves. The low-field mobility showed a great dependence of L_{LD}/L ratio, increasing with the increase of lightly doped region length. Also, transistors with larger L_{LD}/L ratios present large mobility degradation after the maximum transconductance value, which is attenuated for higher gate voltages, due to its reduced electric field. In order to reproduce analytically this behavior, the quadratic attenuation factor θ_2 has shown to present negative values. By using the extracted low-field mobility and degradation factors from experimental GCSOI, an analytical model of uniformly doped SOI MOSFET has been used in a SPICE simulator and was able to reproduce the experimental data with a percentage error smaller than 7.91% for low V_{DS} and 15% for high V_{DS} after transconductance peak, whereas in [5] it has a 6.8% of error, what validates this simulation strategy from the mobility point of view.

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