

Drain Current and Short Channel Effects Modeling in Junctionless Nanowire Transistors

Renan D. Trevisoli, Rodrigo T. Doria, Michelly de Souza, and Marcelo A. Pavanello

Department of Electrical Engineering, Centro Universitario da FEI, Sao Bernardo do Campo, Brazil
e-mail: renantd@fei.edu.br

ABSTRACT

Junctionless nanowire transistors (JNTs) are considered promising for the sub-20 nm era, since they provide a great scalability without the need for rigorously controlled doping techniques. In this work, the modeling of triple-gate JNTs is addressed, focusing on the short-channel effects. Analytical expressions for the subthreshold slope, threshold voltage roll-off and drain induced barrier lowering are presented. The model is validated using tridimensional numerical simulations.

Index Terms: Junctionless Nanowire Transistors, Analytical Model, Subthreshold Slope, Drain Induced Barrier Lowering.

I. INTRODUCTION

Planar MOS devices miniaturization becomes quite challenging for transistors with reduced channel length due to the loss of gate control over the channel charges. As an alternative, multi-gate devices have been developed due to the better electrostatic control of the charges, which leads to a reduction of the short-channel effects [1-6]. However, for devices with extremely reduced channel length, it is needed the formation of ultra-sharp junctions with a high process complexity at source/channel and drain/channel interfaces. In order to address this issue, Junctionless Nanowire Transistors (JNTs) have been proposed [7-11] and have been the focus of several recent studies [12-18].

The JNT is a heavily-doped silicon nanowire surrounded by the gate stack. The doping distribution is constant from source to drain with the same doping element and concentration. Therefore, there are no doping gradients, eliminating impurity diffusion-related problems [7]. For an nMOS device an n-type element is used, whereas a p-type dopant is used in a pMOS device. The Junctionless transistor works similarly to an accumulation mode SOI device (AMSOI) [19]. For gate voltages (V_G) lower than the threshold voltage (V_{TH}), the silicon nanowire is fully depleted such that there is only a small drain current due to the diffusion of carriers. For gate voltages slightly higher than V_{TH} , the current flows through drift in a neutral channel at the center of the device whereas for V_G higher than the flatband voltage (V_{FB}), the current flows through both

an accumulation layer and bulk conduction. However, as stated by Kranti *et al.* [20], the JNT operates mainly in the partial depletion regime with a reduced electric field [21], while the AMSOI works most of time in accumulation regime with a higher electric field. Also, the bulk current in JNTs is higher than in the AMSOI owing to the heavier doping concentration. A schematic view of a triple-gate JNT is presented in Fig. 1, where the silicon nanowire height (H) and width (W), the gate oxide thickness (t_{ox}), the channel length (L) and the buried oxide thickness (t_{Box}) are indicated.

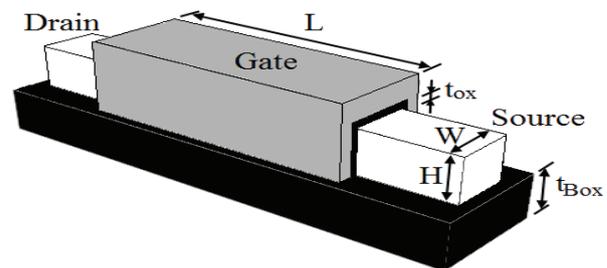


Figure 1. Schematic view of a triple-gate Junctionless Nanowire Transistor.

The modeling of junctionless devices has been the focus of several recent studies [14-15,22-23], however, most of them are based on cylindrical, double-gate or planar devices. In this work, an analytical model for triple-gate devices is derived from the solution of the Poisson equation for long channel devices and a correction for short channel effects is included in the model.

Analytical expressions for the subthreshold slope (S), threshold voltage roll-off ($V_{TH,roll-off}$) and drain induced barrier lowering (DIBL) are also proposed.

II. LONG-CHANNEL DRAIN CURRENT MODEL DERIVATION

In Fig. 2, a representation of the longitudinal section of a n-type JNT is presented, considering that the biases V_G and V_D are applied at the gate and at the drain (the source is grounded), respectively. In the region between $0 \leq y \leq A$, there is the conduction through both accumulation layer and bulk whereas for $A < y \leq B$ there is only bulk conduction. In case of $A = L$, the whole channel present an accumulation layer whereas if $A = 0$, there is only the bulk conduction. If $B = L$, there is no pinch-off, i.e. the device is not in saturation. For B lower than L , there is a depletion region between the drain and the channel, which is induced by the drain potential, similarly to an inversion-mode device. The distance between B and L leads to a reduction

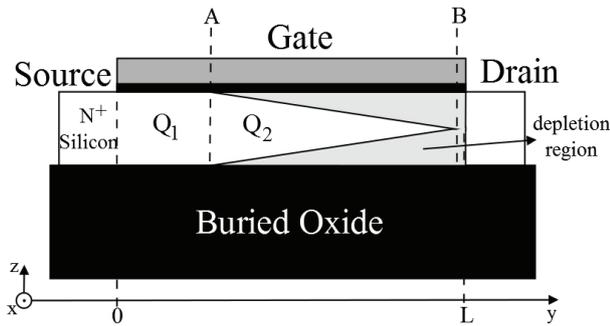


Figure 2. Longitudinal-section of a Junctionless Nanowire Transistor.

of the effective channel length which is modulated by the drain bias. This variation of B degrades (increases) the output conductance of the devices and is especially important for short-channel transistors.

The drain current can be obtained using the equation:

$$I_D = \mu_n Q \frac{dVy}{dy}, \quad (1)$$

where μ_n is the electron mobility, Q is conduction charge per unit of length and Vy is the voltage at a point y along the channel.

From Fig. 2, it can be seen that the charge Q can be considered separately in each region of the device depending on the conduction regime: Q_1 for $0 \leq y \leq A$ and Q_2 for $A < y \leq B$. Thus, the drain current can be obtained through the integration of (2), where the first term results in the current I_1 whereas the second results in I_2 . The sum $I_D = I_1 + I_2$ is the total drain

current that flows through the device. The voltages V_A and V_B represent the voltages at the points A and B, respectively.

$$I_D = \frac{\mu_n}{L} \int_0^{V_A} Q_1(y) dVy + \frac{\mu_n}{L} \int_{V_A}^{V_B} Q_2(y) dVy = I_1 + I_2. \quad (2)$$

The charge density per unit of length Q_1 , which is related to the conduction in both accumulation layer and body, can be described as

$$Q_1 = Q_t + C_{ox}(V_G - V_{FB} - Vy), \quad (3)$$

where $Q_t = (q \cdot N_D \cdot H \cdot W)$, N_D is the donor doping concentration, C_{ox} is the gate capacitance per unit of length and q is the electron charge. The second term of (3) represents the accumulation layer formed at the interface silicon/gate oxide whereas the first one is related to the bulk charge.

Eq. (3) can be integrated from 0 to V_A as shown in (2), resulting in the component I_1 of the current:

$$I_1 = \frac{\mu_n}{L} \left(Q_t V_A + C_{ox}(V_G - V_{FB})V_A - \frac{V_A^2}{2} \right). \quad (4)$$

In order to obtain the charge Q_2 , which is related only to bulk conduction, the two-dimensional Poisson equation must be solved:

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dz^2} = -\frac{q N_D}{\epsilon_{Si}}, \quad (5)$$

where Φ is the potential, x and z are the axes in width and height directions, respectively, and ϵ_{Si} is the silicon permittivity. The carrier density has been neglected in (5) once the bulk charge is controlled by the depletion.

The approximation that the potential varies similarly in both x and z directions ($d\Phi/dx = d\Phi/dz$) has been used in order to solve (5). This approximation has already been used in [24-26]. The center potential at the source side of the device has been considered as zero, since it is connected directly to the ground (no junctions). The electric field has also been considered as zero at the center. Eq. (5) can be integrated following these boundary conditions such that the depletion charge (Q_{Depl}) can be obtained by [24]

$$Q_{Depl} = 2\alpha \left[\frac{-1}{C_{ox}} + \sqrt{\left(\frac{1}{C_{ox}}\right)^2 + \frac{(V_{FB} - V_G + Vy)}{\alpha}} \right], \quad (6)$$

where $\alpha = \epsilon_{Si} q N_D (2H + W)^2/4$.

The total bulk conduction charge can be obtained by the difference of the charge Q_t and the de-

pleted charge ($Q_2 = Q_t - Q_{D_{epi}}$). Therefore, the charge Q_2 can be integrated as shown in (2), resulting in the component I_2 of the drain current

$$I_2 = \frac{\mu_n}{L} (V_B - V_A) \left(\frac{2\alpha}{C_{ox}} + Q_t \right) - \frac{\mu_n}{L} \frac{4\sqrt{\alpha}}{3} \left((V_{FB} - V_G + V_B) + \frac{\alpha}{C_{ox}^2} \right)^{1.5} + \frac{\mu_n}{L} \frac{4\sqrt{\alpha}}{3} \left((V_{FB} - V_G + V_A) + \frac{\alpha}{C_{ox}^2} \right)^{1.5} \quad (7)$$

III. VOLTAGES V_A AND V_B

The voltage at the point V_A represents the transition between the bulk conduction regime and the accumulation layer plus bulk conduction regime. This transition occurs around $V_y = V_G - V_{FB}$ for $V_G > V_{FB}$. For $V_G < V_{FB}$ there is only bulk conduction, which means that V_A equals the source voltage (V_S) in this condition. For $V_G > V_{FB}$, an accumulation layer is formed at least at the source side of the channel and, depending on V_G and V_D , this accumulation layer may extend through the whole channel. The maximum value that the voltage at the point A may assume is V_B , which would mean that the accumulation layer is formed from source to drain. Therefore, V_A can vary between two well-defined points (V_S and V_B) depending on the applied biases. In order to have a smooth transition between bulk and accumulation layer regimes, equation (8) has been used for V_A , where A_1 controls the smoothness and have been set to 6.

$$V_A = V_S + \frac{V_B}{(1 + A_1 \exp(-A_1(V_G - V_{FB})))^{1/2}} \quad (8)$$

The voltage at the point B represents the effective drain-source voltage ($V_{D_{Se}}$), which values V_D until the device reaches saturation. Therefore, to limit the maximum $V_{D_{Se}}$ in the saturation voltage ($V_{D_{sat}}$), the smooth function was used:

$$V_{D_{Se}} = V_B = V_{D_{sat}} \left[1 - \frac{\ln[1 + \exp(A_2(1 - V_D/V_{D_{sat}}))]}{\ln(1 + \exp(A_2))} \right] \quad (9)$$

where A_2 is a fitting parameter that controls the transition from triode to saturation and has been set to 4.

To obtain the saturation voltage, the relation $I_{D_{sat}} = Q_{sat} \cdot v_{sat}$, where $I_{D_{sat}}$ is the saturation current, Q_{sat} is the charge density per unit of length in the saturation condition and v_{sat} is the velocity saturation, has been used [27]. Combining equations (4), (6) and (7) with the saturation relation, $V_{D_{sat}}$ can be obtained through the solution of the polynomial equation:

$$K_3 \cdot w^3 + K_2 \cdot w^2 + K_1 \cdot w + K_0 = 0, \quad (10)$$

where $K_3 = -4i_n \sqrt{\alpha} (3L)$, $K_2 = i_n (2\alpha / C_{ox} + Q_t) / L$, $K_1 = 2v_{sat} \sqrt{\alpha}$ and

$$K_0 = \frac{i_n}{L} \left[\frac{4}{3} \frac{\alpha^2}{C_{ox}^3} - \left(\frac{2\alpha}{C_{ox}} + Q_t \right) \left(\frac{\alpha}{C_{ox}^2} + \frac{L v_{sat}}{i} \right) + Q_t (V_G - V_B) + \frac{C_{ox}}{2} (V_G - V_B)^2 \right]$$

The saturation voltage is obtained by

$$V_{D_{sat}} = w - V_{FB} + V_G - \alpha / C_{ox}^2. \quad (11)$$

It is worth mentioning that the minimum saturation voltage has been limited in the thermal voltage (ϕ_t) as in a planar MOSFET [28]. For the subthreshold regime, it was considered that the current presents an exponential dependence on the gate voltage, calculated by

$$I_D = (I_1 + I_2) \exp((V_{GS} - V_G) / (n\phi_t)), \quad (12)$$

where n is the body effect factor, which is close to the unit for JNTs, and V_{GS} is the voltage applied between the gate and the source.

In (12), a smooth function is used to the voltage V_G in order to guarantee the continuity of the current at the transition between subthreshold and above threshold regions, described by

$$V_G = V_{TH} + V_{TH} \frac{\ln[1 + \exp(A_3(V_{GS}/V_{TH} - 1))]}{\ln(1 + \exp(A_3))}, \quad (13)$$

where A_3 controls the transition and has been set to 12 and V_{TH} is calculated by [24]

$$V_{TH} = V_{FB} - qN_D \left[\frac{WH}{C_{ox}} + \frac{1}{\epsilon_{Si}} \left(\frac{WH}{(2H+W)} \right)^2 \right] \quad (14)$$

IV. MODEL VALIDATION FOR LONG-CHANNEL DEVICES

In order to validate the model for long channel devices, three-dimensional TCAD simulations of n-type devices have been performed with Synopsys tools [29-30]. The simulated JNTs present nanowire height and width of 10 nm, gate oxide thickness of 2 nm, doping concentration of $N_D = 1 \times 10^{19} \text{ cm}^{-3}$ and channel length of 1 μm . P⁺ polysilicon has been used as gate material. The low field mobility has been considered constant and equal to 100 cm^2/Vs .

In Fig. 3, the drain current in linear and logarithm scales and the transconductance ($g_m = dI_D/dV_G$) are presented as a function of the gate voltage for several drain biases. From this figure, it is clear that the drain current and its derivative are correctly predicted by the model in both subthreshold and above thresh-

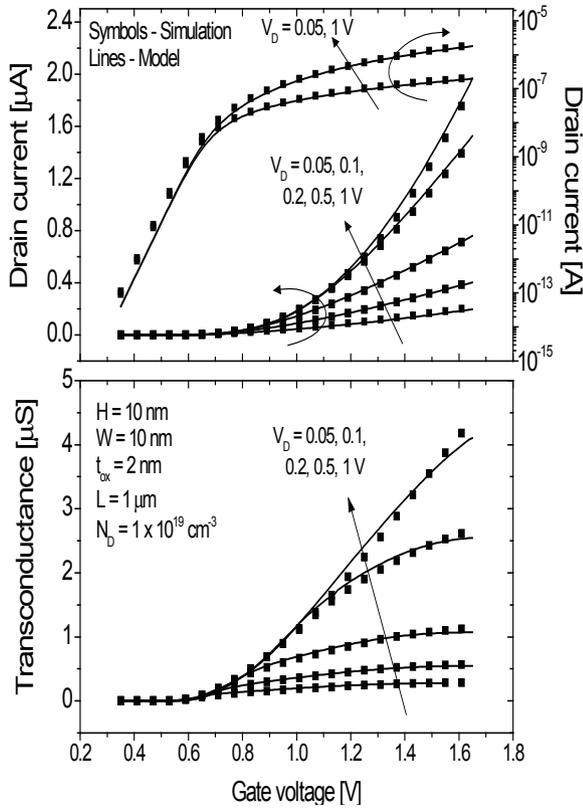


Figure 3. Drain current and transconductance as a function of the gate voltage for the n-type devices.

old regions. In Fig. 4, the drain current and the drain output conductance ($g_D = dI_D/dV_D$) are presented as a function of the drain voltage for several gate overdrive voltages ($V_{GT} = V_G - V_{TH}$). From this figure, it can be concluded that the model adequately predicts the characteristics for long channel devices.

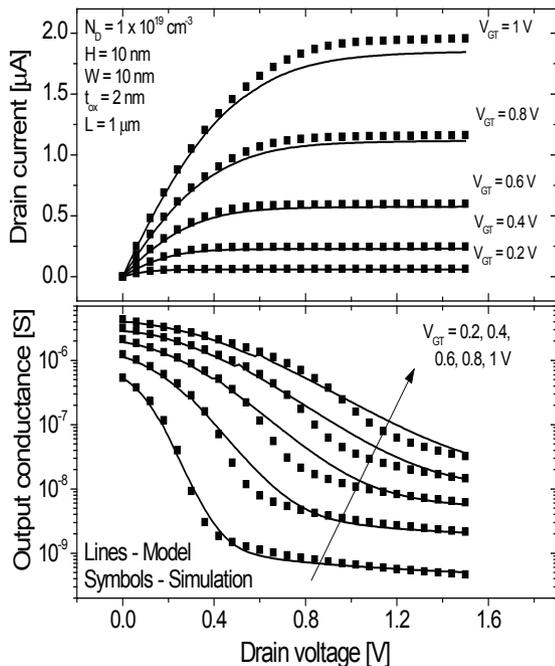


Figure 4. Drain current and output conductance as a function of the drain voltage for the n-type devices.

The model has been also compared to experimental data. The devices were fabricated according [7] and present $H = t_{ox} = 10$ nm, doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and an effective width of 20 nm. The low field mobility has been calculated considering the lattice and ionized impurities scattering [31] and carrier-carrier scattering [32]. The series resistance has been taken into account iteratively considering source/drain length of 150 nm each. In Fig. 5, the drain current (A) and the transconductance (B) are presented as a function of the gate voltage for different temperatures ranging between room temperature up to 470 K. In order to take the incomplete carrier ionization into account, which is very important for these devices [18,24,33-34], the model proposed by Altermatt *et al.* [35] has been used, such that the doping concentration has been substituted by the ionized doping concentration. From this Fig. 5, it is clear that the model describes adequately the dependence on the temperature.

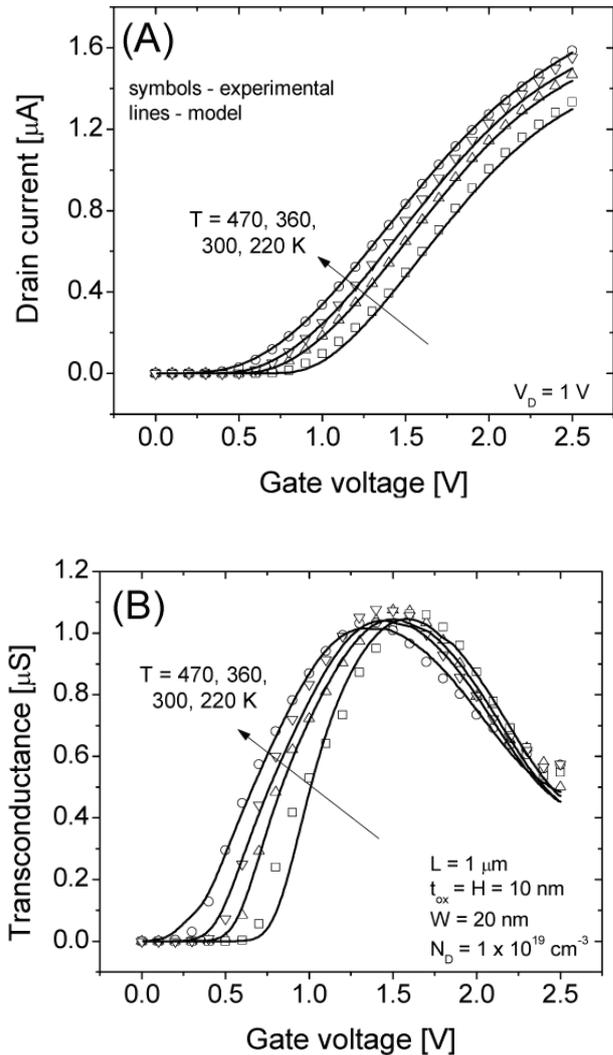


Figure 5. Drain current (A) and transconductance (B) as a function of the gate voltage comparing experimental and modeled data for different temperatures.

V. SHORT-CHANNEL EFFECTS CORRECTION

In order to obtain an analytical expression which accounts for short-channel effects, the tridimensional Poisson equation must be solved:

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dz^2} + \frac{d^2\Phi}{dy^2} = -\frac{qN_D}{\epsilon_{Si}} \quad (15)$$

In order to find an analytical solution for (15), the superposition principle can be used, such that the solution is obtained by the sum of the solution of (5) with the solution of the 3D Laplace equation given by

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dz^2} + \frac{d^2\Phi}{dy^2} = 0 \quad (16)$$

The solution of (16) for the minimum potential in the channel is given by [1,26,36]

$$\Phi_{min} = \frac{V \sinh(y_{min}/\lambda) + U \sinh((L - y_{min})/\lambda)}{\sinh(L/\lambda)} \quad (17)$$

where λ is characteristic length, which for a triple gate device can be obtained through the average of the two scaling lengths (λ_1 related to the width scaling and λ_2 related to the height one) [1], y_{min} is the point of the minimum potential in the channel given by (18) [36],

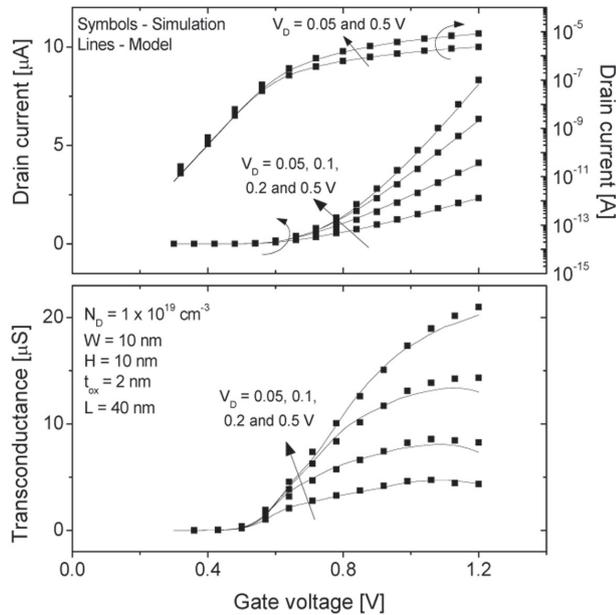


Figure 6. Drain current and transconductance as a function of the gate voltage for a short-channel device ($L = 40$ nm).

$U = -\Phi_{2D}$, $V = V_D - \Phi_{2D}$ and Φ_{2D} is the potential obtained from the solution of the 2D Poisson equation.

$$y_{min} = \frac{\lambda}{2} \ln \left[\frac{U \exp(L/\lambda) - V}{V - U \exp(-L/\lambda)} \right] \quad (18)$$

The surface potential Φ_{2D} for the depletion region can be obtained through eq. (6) leading to

$$\Phi_{2D,depl} = V_G - V_{FB} - \frac{\alpha}{2C_{ox}^2} + \sqrt{\frac{\alpha}{C_{ox}^2} \sqrt{\frac{\alpha}{4C_{ox}^2} - (V_G - V_{FB})}} \quad (19)$$

In Figs. 6 and 7 the drain current and its derivative are presented as a function of the gate and drain biases, respectively, comparing simulated and modeled data for short channel-devices. From these curves, it can be seen that the inclusion of eq. (17) adequately describes the short channel effects in the drain current.

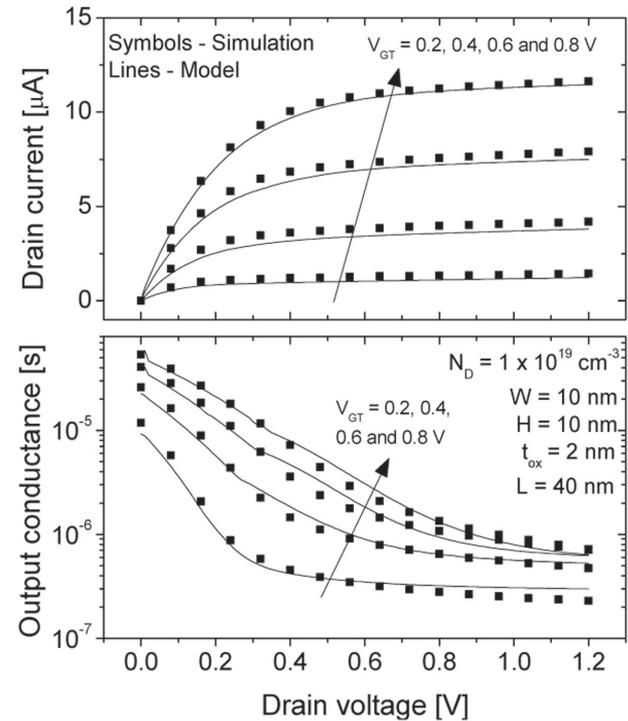


Figure 7. Drain current and output conductance as a function of the drain voltage for a short-channel device ($L = 40$ nm).

VI. SUBTHRESHOLD SLOPE

Eq. (17) can be used to obtain an expression for the subthreshold slope dependence on the channel length. In order to develop this expression the variation of the minimum potential in the channel with the gate voltage needs to be analyzed. In Fig. 8, the point of the minimum potential normalized by the channel length is shown as a function of the gate voltage for devices with different L at a low drain bias. The thresh-

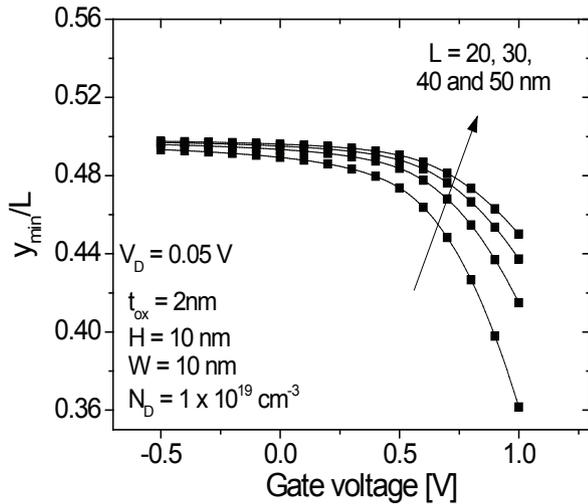


Figure 8. Point of the minimum potential in the channel normalized by the channel length as a function of the gate voltage.

old voltage is about 0.65 V for these devices. From this figure, one can note that for $V_G \ll V_{TH}$, the point of the minimum potential tends to the half of the channel length ($y_{min}/L = 0.5$). This is related to the small difference between the potential barriers at source and drain. Therefore, in order to derive an expression for S , the point y_{min} can be considered as $L/2$. With this approximation, eq. (17) can be rewritten in the subthreshold regime for a low drain bias as

$$\Phi_{\min,sub} = \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)}(V + U). \quad (20)$$

In Fig. 9, the minimum potential obtained from (18) is presented as a function of the gate voltage for the devices with different channel lengths. From this figure it is clear that $\Phi_{\min,sub}$ varies linearly with the gate voltage in the subthreshold region. It can be also noted that the minimum potential and its variation with V_G increases when the channel length is reduced. The variation of the subthreshold slope (ΔS) with the dimensions of the device is related with the variation of $\Phi_{\min,sub}$ with V_G :

$$\Delta S = S \left(\frac{d\Phi_{\min,sub}}{dV_G} \right). \quad (21)$$

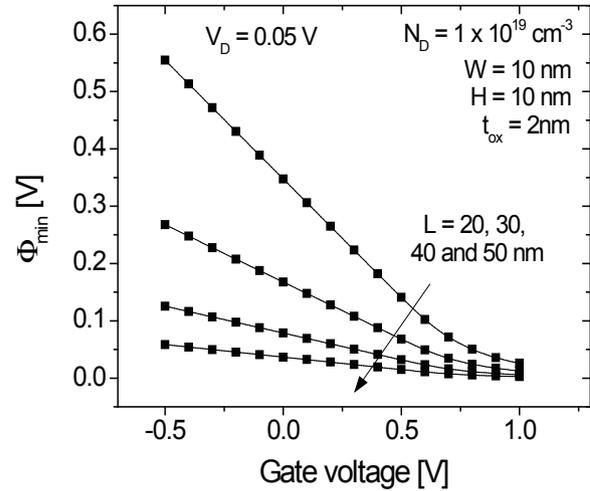


Figure 9. Minimum potential in the channel as a function of the gate voltage for devices of different lengths.

where S was calculated by $S = (kT/q) \ln(10)n$, with $n \approx 1$.

Differentiating (20) in relation to the gate voltage it can be obtained

$$\frac{d\Phi_{\min,sub}}{dV_G} = \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)} \frac{d(2\Phi_{2D})}{dV_G}. \quad (22)$$

In the subthreshold regime, the surface potential varies linearly with the gate voltage ($\Phi_{2D} \propto V_G$), since all the charges in the channel are depleted, so that there is no charge variation with V_G [15,26]. Therefore, the subthreshold slope considering short-channel effects can be calculated by

$$S_{SCE} = S + \Delta S = S \left(1 + 2 \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)} \right). \quad (23)$$

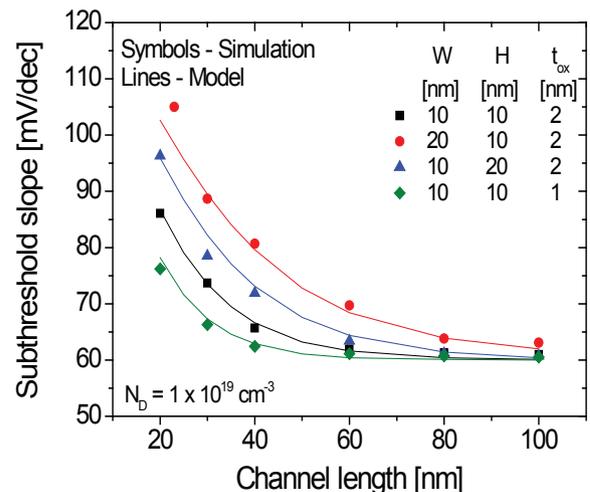


Figure 10. Subthreshold slope as a function of the channel length comparing modeled and simulated data.

The subthreshold slope calculated by (23) has been compared to the data of simulated devices of different dimensions in Fig. 10. From this figure, one can conclude that eq. (23) can predict adequately the subthreshold slope on the devices characteristics.

VII. THRESHOLD VOLTAGE ROLL-OFF AND DRAIN INDUCED BARRIER LOWERING

Eq. (17) can also be used to develop an analytic model for the threshold voltage roll-off and for the drain induced barrier lowering. To obtain an analytical expression for the V_{TH} roll-off, the surface potential in the threshold condition is needed. For a long device, this potential can be obtained by [24]

$$\Phi_{V_{th}} = \frac{q N_D}{\epsilon_{Si}} \left(\frac{WH}{2H+W} \right). \quad (24)$$

However, this potential changes with the variation of the minimum potential in the channel. Therefore, the potential at threshold considering short-channel effects ($\Phi_{V_{th},SCE}$) can be obtained by the difference between the surface potential for long-channel devices and the minimum potential in the surface in the threshold condition

$$\Phi_{V_{th},SCE} = \Phi_{V_{th}} - \Phi_{min,V_{th}}. \quad (25)$$

Considering that the threshold voltage is extracted with a low drain bias, the point of the minimum potential in the channel occurs in the center of the device ($y_{min} = L/2$, as shown in Fig. 8). The potential $\Phi_{min,V_{th}}$, which represents the threshold voltage roll-off ($V_{TH,roll-off} = \Phi_{min,V_{th}}$) can be obtained by eq. (20) with $U = \Phi_{2DV_{th},SCE}$, $V = V_D + \Phi_{2DV_{th},SCE}$:

$$\Phi_{min,V_{th}} = (2\Phi_{V_{th},SCE} + V_D) \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)}. \quad (26)$$

If the drain bias is much lower than the surface potential, eq. (26) can be rewritten as

$$\Phi_{min,V_{th}} = 2\Phi_{V_{th},SCE} \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)}. \quad (27)$$

Substituting (27) in (25), the potential at threshold considering short-channel effects is described by

$$\Phi_{V_{th},SCE} = \frac{\Phi_{V_{th}}}{1 + 2 \frac{\sinh(L/(2\lambda))}{\sinh(L/\lambda)}}. \quad (28)$$

The threshold voltage roll-off is finally obtained substituting (28) in (27), which leads to

$$V_{TH,roll-off} = \frac{\Phi_{V_{th}}}{1 + \frac{\sinh(L/\lambda)}{2\sinh(L/(2\lambda))}}. \quad (29)$$

In Fig. 11, the $V_{TH,roll-off}$ obtained through eq. (29) is compared to the one extracted from the simulated devices. For the simulated devices, V_{TH} is extracted using the double-derivative method [37] for a drain bias of 50 mV. The comparison is performed for devices of different dimensions, showing that the model is adequate for predict the $V_{TH,roll-off}$.

The drain induced barrier lowering can be calculated using the threshold voltage roll-off. Firstly, the surface potential Φ_{2D} is calculated for $V_G = V_{TH} - V_{TH,roll-off}$ using eq. (19), with V_{TH} obtained by (14).

Then, the point y_{min} is calculated considering a higher drain bias, e.g. $V_D = 1$ V, using (18) and the minimum potential at this higher V_D ($\Phi_{min,V_D=1V}$) is obtained by (17). The drain induced barrier lower is calculated as

$$DIBL = \Phi_{min,V_D=1V} - V_{TH,roll-off} + DIBL_L. \quad (30)$$

where $DIBL_L$ is the drain induced barrier lowering extracted for the long device.

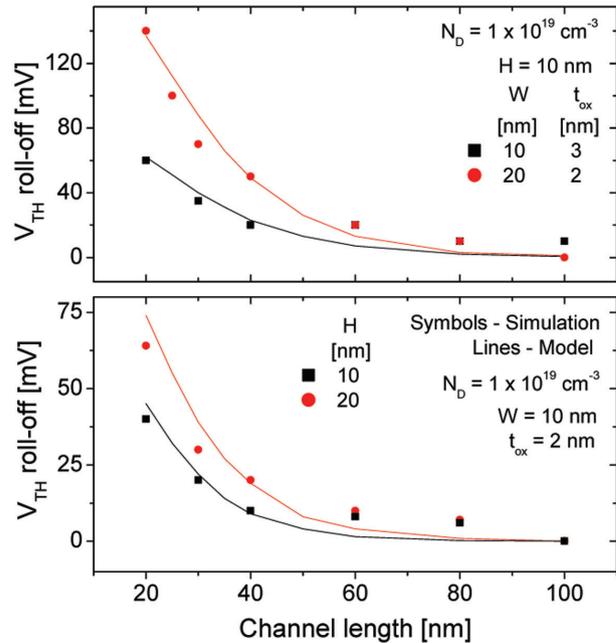


Figure 11. Threshold voltage roll-off comparing modeled and simulated data for devices of different dimensions.

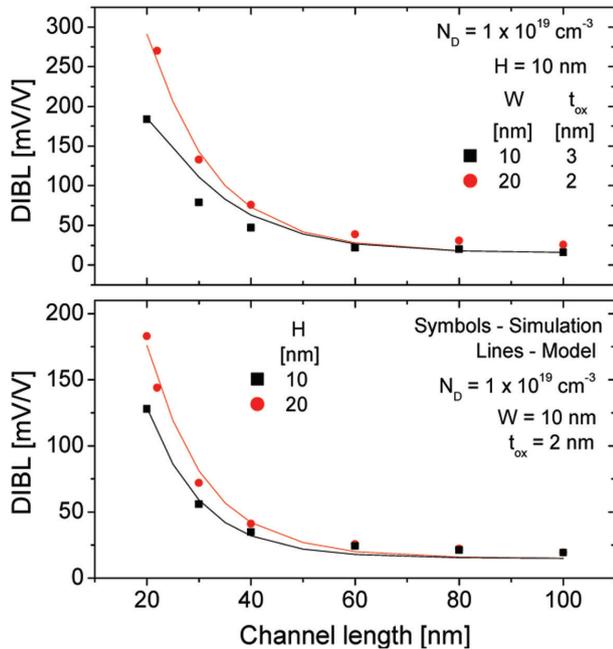


Figure 12. Drain induced barrier lowering as a function of the channel length comparing modeled (lines) and simulated (symbols) data for devices of different dimensions.

In Fig. 12, the DIBL values calculated by eq. (30) as described above are compared to the ones extracted from the simulated devices. JNTs of different dimensions have been considered. The values of $DIBL_L$ is 15 mV/V for all the studied devices and can be considered just as an adjust parameter. From this figure it is clear that the model accurately predicts the DIBL in short-channel devices.

VIII. CONCLUSIONS

This work proposes a drain current model for triple-gate junctionless nanowire transistors, which has been derived from the solution of the 2D Poisson equation. The saturation voltage has also been addressed. This model is compared to the results of three-dimensional TCAD simulations and experimental measurements. A parameter for the short-channel effects correction in the drain current model has also been presented. In this case, the validation is performed through the 3D simulations. Using the short-channel effects correction term, expressions for the subthreshold slope, threshold voltage roll-off and drain induced barrier lowering have been derived. These equations have also been compared to simulated data for devices of different dimensions, showing an excellent agreement.

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