A customized genetic algorithm with in-loop robustness analyses to boost the optimization process of analog CMOS ICs

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ABSTRACT

The traditional optimization processes of analog complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) are very complex, slow, and based on the designers' experience. To obtain robust potential solutions, it is necessary to perform robustness analyses (RAs) through SPICE simulations. However, this approach represents a huge bottleneck in the optimization processes due to the significant increase of time of the SPICE simulations concerning the RAs. Therefore, this work proposes an innovative customized genetic algorithm (GA) to boost the optimization process of analog CMOS ICs. The main results obtained showed that all designs of analog CMOS ICs reached a yield of 100% and a remarkable reduction of the optimization time (from 23% to 79%) in comparison with the standard optimization process with the GA, without reducing the random samples number considered in the RAs, and consequently preserving their robustness accuracy.

1. Introduction

The continuous downscaling of the complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) technologies increases the variability of dimensional and technological parameters of the metal-oxide-semiconductor field effect transistors (MOSFETs) due to the random placement of dopant in the channel region, roughness of the edges of the gate region (induced by the gate etching and lithography processes), oxide thickness fluctuations which affect the mobility of mobile charge carriers in the channel (μ_0), threshold voltage (V_{th}), etc. [1]. Therefore, after the manufacturing process, the electrical performance of the analog CMOS ICs can be severely impaired [1].

As a consequence of the enormous number of design specifications (figures of merit) that must be achieved at the same time, the traditional optimization processes of the analog CMOS ICs are very complex, demanding a high design cycle time, and therefore they are mainly based on the knowledge and experience of the designers [2–4]. This situation is further aggravated by the effects of manufacturing processes' variations regarding the nanoscaled technology nodes [2,3].

For many years, most of the design tools for analog CMOS ICs [5,6] have only taken into account some extreme global variations of dimensional and technological parameters of MOSFETs in relation to the manufacturing processes and environmental conditions through the corner analysis (CA) [7,8]. However, in the most sophisticated

technology nodes (below 130 nm), the local variations in the dimensional and technological parameters of the MOSFETs, regarding the minimum dimensions allowed by the CMOS ICs manufacturing processes, have caused a higher impact on the electrical performance of analog CMOS ICs, mainly in relation to their robustness [7]. To overcome the limitations of the accuracy of the figures of merit (FoMs) obtained through SPICE simulations regarding the CAs, the Monte Carlo analysis (MCA) is currently the most used for designing analog CMOS ICs [8]. Nevertheless, the use of MCA for designing the analog CMOS ICs results in a significant increase in the design cycle time [8].

The analog CMOS IC is classified as a system of multiple input variables and many output variables. The manual traditional design methods by using SPICE simulations are complex, need several interactions between the designers and simulations and consequently they are very time consuming [4]. To overcome these issues, the evolutionary algorithms (EAs) of the artificial intelligence have been used to optimize these types of circuits with great success [4,5,9–12]. The EAs are classified into two main categories: I) *A priori*: it is characterized by the definition of desired specifications before the execution of the optimization process. This approach transforms a multi-objective problem into a single-objective problem by using a fitness function which is responsible for assigning a value to each potential solution (input variables such as the MOSFETs dimensions, bias conditions, etc.) taking into account its multiple objectives found by the evolution process. The potential solution that

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                          ┌─────────────────────┐
                          │  Evolution process  │
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(A) Configuration of the MTGSPICE

(B) DC evolution process (first evolution stage)

(C) AC evolution process (second evolution stage)

(D) If repeated potential solutions exist, replace them by random potential solutions

(E) SPICE simulations for each potential solution of the population

(F) Calculation of the values of the fitness functions

(G) Are there potential solutions? — Potential solutions that meet the nominal desired specifications

No / Yes

(H) SPICE simulations regarding the corner analysis and/or Monte Carlo analysis

(I) Are there robust potential solutions? — No

Yes

(J) Save the most robust potential solutions found of the current generation that will be used in the next generation

(K) Robustness driven elitism

(L) Save the data log and update the graphs regarding the most robust potential solution of the current generation in the MTGSPICE

(M) Selection, crossover, and mutation processes — New solutions (new generation)

(N) Is the stop criterion reached? — No / Yes

Specifications achieved? (first stop criterion)

Maximum number of generations (second stop criterion)

(O) Save and show the potential robust solutions requested by the designer

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Legend:
- Typical SPICE simulations (Nominal)
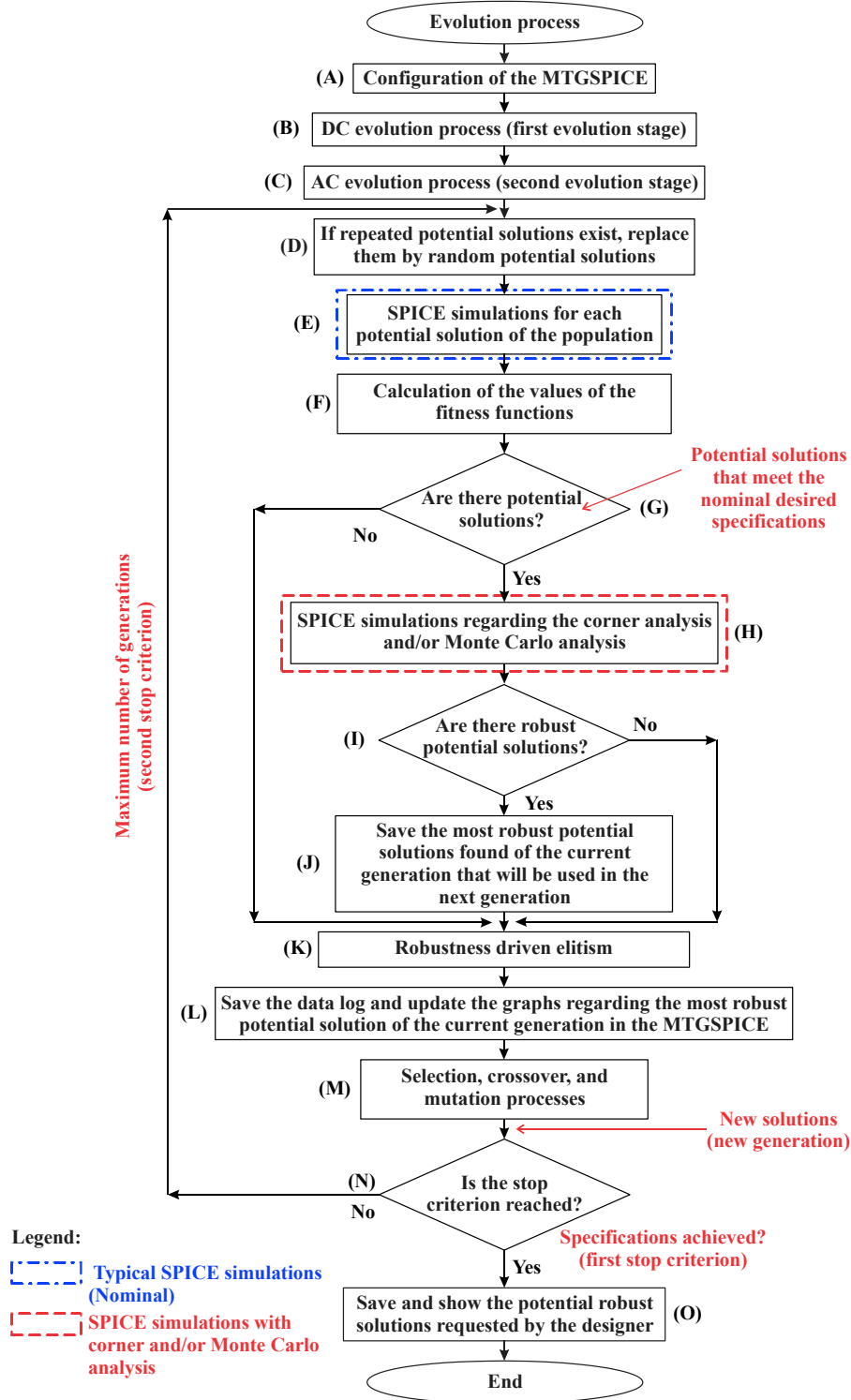- SPICE simulations with corner and/or Monte Carlo analysis

Fig. 1. Flowchart of the customized GA optimization process.

presents the highest value of the fitness function corresponds to the one which better meets all the desired specifications (FoMs) at the same time. An example of this approach is the standard genetic algorithm (GA) [13]; II) *A posteriori*: it can provide an enormous set of potential solutions that can meet the desired specifications. However, the designers are in charge of choosing the solution that best suit their needs [13]. This methodology is usually based on the Pareto techniques, such as the nondominated sorting genetic algorithm II (NSGA-II) and strength Pareto evolutionary algorithm (SPEA) [13]. Some recent works related to analog CMOS ICs

optimizations have used *a posteriori* approaches, such as the NSGA-II [9–11]. However, they are often unable to explore potential solutions in specific regions of the Pareto front by using modest computational resources [12]. Furthermore, the designer has great difficulties to choose a potential solution which presents the best tradeoff among the different desired design specifications [13]. Therefore, the *a priori* approach through the use of normalized exponential fitness functions becomes an alternative approach to overcome the drawbacks mentioned in the *a posteriori* technique, focusing on analog CMOS ICs designs [12,14]. In this
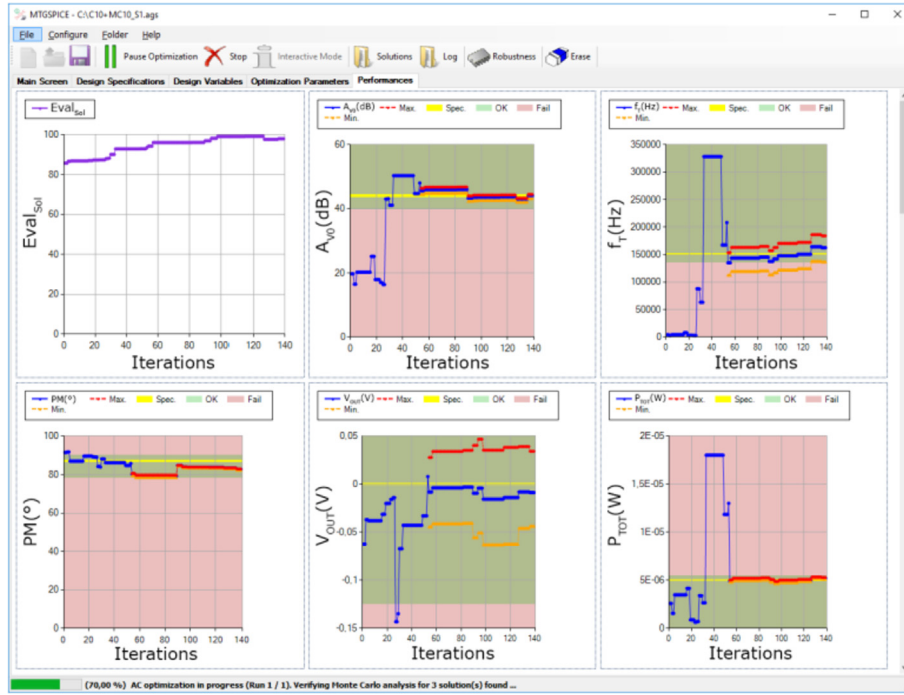
Fig. 2. Monitoring of the design parameters in the MTGSPICE, taking into account the CA and/or MCA in the loop of the optimization process.
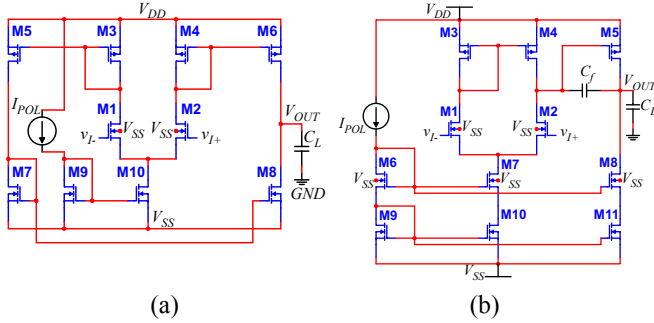

Fig. 3. Topologies of the CMOS OTAs used in this work: (a) SESS and (b) CBMC.

Table 1

Desired Design Specifications of the μP_SESS and HG_CBMC OTAs.

Design Specifications	μP_SESS	HG_CBMC
Open loop voltage gain (A_{V0})	≥44 dB	≥70 dB
Unit voltage gain frequency (f_T)	≥150 kHz	≥44 kHz
Phase margin (PM)	≥87°	≥67°
DC output voltage (V_{OUT})	±125 mV	±50 mV
Power consumption (P_{TOT})	≤5 μW	≤484 nW
Gate area of the MOSFETs (A_G)	≤8636 μm²	≤8636 μm²

Table 2

Optimization Parameters of the μP_SESS and HG_CBMC OTAs.

Design Parameter	Range	
	μP_SESS	HG_CBMC
W	[1, 500, 0.35] μm	[1, 10, 0.1] μm
L	[1, 20, 0.35] μm	[0.7, 7, 0.05] μm
I_{POL}	[0.01, 1, 0.01] μA	[10, 500, 1] nA
C_f	–	[1, 100, 0.05] pF

Note: "Range" indicated in this Table is related to the minimum and maximum values, and the value of the step that was adopted for these parameters to perform the optimization process.

work, we have used the Gaussian-based exponential fitness functions proposed in Ref. [14] to improve the robustness and effectiveness of the optimization processes of analog CMOS ICs designs based on *a priori* techniques.

Usually, the professional (commercial) Electronic Design Automation (EDA) tools for the optimization of analog CMOS ICs do not consider the SPICE simulations with the robustness analysis (RA: CA and MCA) in the loop of the optimization process due to the enormous number of simulations to be performed [15,16], resulting in an extensive increase in the time of the optimization process [9,17]. We could observe that these professional computational tools use several different techniques to reduce the impact of RA in the optimization processes of analog CMOS ICs. Most of them are based on the reduction of the number of samples

used to perform the MCA, such as Latin hypercube sampling (LHS) and quasi-Monte Carlo (QMC) [8,18,19], approximations (k-means [9]) or by using simplified models (kriging [3]) to estimate the results of MCA. Although these approaches help to reduce the optimization time, when they are compared with the results obtained by the conventional MCA, we can observe that they reduce the accuracy of the robustness study of the analog CMOS ICs [20].

In this context, the main goal of this work is to reduce the impact of the SPICE simulations considering the RA (SS_{RA}) in the loop of the optimization process of the analog CMOS ICs, without reducing the number of samples of the RA [8] and without using metamodel techniques to predict the behavior of the RA [3] in order to guarantee a better accuracy in the robustness study of analog CMOS ICs designs to be implemented. This novel methodology is performed by using an in-house optimization tool named MTGSPICE [14], which will implement a customized GA with the following features: I- the RA is included in the loop of the optimization processes; II- the values of the fitness functions of the FoMs obtained through SPICE simulations are defined by taking into account their robustness, which are obtained through the RA. It is important to highlight that the nominal value of each FoM is obtained through SPICE simulations regarding direct current (DC) and alternating current (AC) analyses, and its robustness is calculated by the average value of the relative errors considering the minimum and maximum values of each FoM in relation to the desired specifications; III- the elitism

Table 3
Optimization cycle time for the µP_SESS and HG_CBMC OTAs, regarding the in-loop robustness analysis.

N_{CA} and/or N_{MCA}	µP_SESS		HG_CBMC	
	OCT (min.)	SD (%)	OCT (min.)	SD (%)
SFFE + MCA				
2	27.5	72.6	83.2	78.8
5	71.3	64.9	184.4	63.2
10	143.7	98.2	345.1	99.0
Average values	80.8	78.5	204.3	80.4
SFFE + MCA + Re				
2	15.0	79.5	34.3	59.7
5	35.3	48.8	81.7	58.4
10	69.7	76.6	151.4	84.1
Average values	40.0	68.3	89.1	67.4
CFFE + MCA				
2	37.1	77.8	72.3	62.3
5	45.9	72.1	114.0	58.7
10	69.3	55.6	160.0	64.8
Average values	50.8	68.5	115.4	61.9
CFFE + MCA + Re				
2	18.6	81.8	34.5	55.0
5	21.9	56.8	62.1	36.2
10	40.2	43.6	101.8	57.7
Average values	26.9	60.8	66.1	49.6
CFFE + CA				
2	15.2	95.1	85.2	82.4
5	7.5	36.0	45.1	140.0
10	12.3	70.6	68.2	64.3
Average values	11.7	67.3	66.2	95.6
CFFE + CA + Re				
2	9.9	96.7	56.4	76.4
5	5.3	35.5	32.2	137.4
10	8.4	75.7	44.1	66.5
Average values	7.9	69.3	44.2	93.4
CFFE + CA + MCA				
2	16.4	85.3	77.0	84.9
5	13.1	23.8	58.5	73.1
10	20.7	27.2	58.6	28.6
Average values	16.8	45.4	64.7	62.2
CFFE + CA + MCA + Re				
2	11.4	84.4	59.4	72.0
5	10.1	23.1	50.1	67.7
10	17.5	25.7	44.1	27.8
Average values	13.0	44.4	51.2	55.8

Table 4
The OCTs regarding the CFFE + CA + MCA + Re approach ($N_{CA}=N_{MCA}=10$), by using ref. [14], and the number of robust solutions obtained by each approach for the µP_SESS and HG_CBMC designs, respectively.

Method	µP_SESS		HG_CBMC	
	OCT (min.)	N° Sol.	OCT (min.)	N° Sol.
CFFE + CA + MCA + Re	17.5	10.0	44.1	10.0
Ref. [14]	795.6	7.0	771.3	2.0

process is responsible for considering the most robust potential solutions found to perform the crossover and mutation processes; IV- implementation of a reuse strategy of the FoMs obtained from the previous generation which will be used in the next generation of the evolution process, aiming to reduce the optimization cycle time; V- limitation of the maximum number of SS_{RA} as a function of the number of robust solutions already obtained.

Two different topologies of operational transconductance amplifiers (OTAs) were considered in this work to qualify the effectiveness of the RA driven optimization process proposed in this study.

This paper is organized as follows. Section 2 gives an overview of the existent solutions for the optimization process of analog CMOS ICs with in-loop robustness analysis. Section 3 presents the robustness driven optimization process implemented in the MTGSPICE ("in house" tool). Next, in Section 4, the OTAs' topologies are described. The OTAs'

specifications, configurations' parameters of MTGSPICE, CA, and MCA are provided in Section 5. Section 6 discusses the main results found in this work. Finally, Section 7 presents the main conclusions of this paper.

2. Related works

Reference [8] proposes to replace the traditional MCA and LHS with QMC simulations to speed up the statistical analysis regarding analog CMOS ICs. The authors compared the QMC method with the MCA and LHS methods. They observed a superior performance of QMC, reducing the computational efforts from 2 to 8 times in relation to the MCA and LHS methods, with an accuracy loss of approximately 1%. The drawback of the QMC approach is the electrical performance degradation of the CMOS ICs for higher dimensionality sampling spaces [9].

Regarding the work described in Ref. [9], the authors have proposed an optimization tool for analog CMOS ICs that uses the traditional MCA without approximations to estimate the yield of the potential solutions considered, during the optimization process. They have proposed the use of the k-means algorithm using a variable number of clusters to select only a few potential solutions to perform the SPICE simulations considering the AC analysis with the MCA (SS_{MCA}). Although they have reported a reduction of up to 91% in the total number of MCAs performed by the optimization process, a compromise was observed between the accuracy of the proposed approach and the number of clusters used during the optimization process. Similarly, the authors in Ref. [17] proposed a methodology (FUZYE) that reduces the total number of MCA that are required in the optimization process of analog CMOS ICs. In each generation of the GA, the population is clustered using the fuzzy c-means (FCM) technique. After that, the MCA was performed for the most representative individual (RI) from each cluster and the yield for the rest of the population was estimated based on the degree of pertinence of FCM and the yield values of the RIs. The results obtained by the FCM approach were compared to a conventional approach, where all individuals of the population were subject to SS_{MCA}. The FCM method achieved a reduction of 89% in the total number of MCA, when compared to the MCA over the full population. Moreover, the proposed FUZYE was compared with the previously proposed k-means clustering algorithm. Although the FCM showed an improvement of up to 13% in yield estimation accuracy in relation to the k-means method, there is a tradeoff between the total number of MCA and the yield estimation accuracy.

In Ref. [21], the authors optimized a two-stage Miller OTA by using a 130 nm Bulk CMOS ICs technology node, by means of an artificial intelligence heuristic approach. They included the desired yield value in the fitness function as one additional design objective. Besides, they proposed a hybrid sampling method to perform the robustness analysis, LHS with a reduced sample size and the conventional random sampling. The hybrid approach was able to reduce the optimization time by 15% in relation to the approach using only the standard MCA.

The work described in Ref. [19] proposed the use of a QMC analysis with adaptive sample size instead of using the traditional MCA in the optimization process of analog CMOS ICs. The objective of this proposal was to reduce the SPICE simulation time required to estimate the yield of the potential solutions of the analog CMOS ICs design. In this case, it was verified that there is a tradeoff between the simulation time and the accuracy of the yield estimation of the potential solutions, which is defined by two parameters: the size of the sample and its increment step. Furthermore, the SPICE simulations taking into account the QMC were not carried out for the infeasible potential solutions in order to boost the efficiency of the optimizer's process. As a reduced number of samples was used during the experiments (between 98 and 128), a more accurate QMC analysis was subsequently performed for the potential solutions obtained with a higher number of samples (from 1081 to 21034) in order to qualify the results obtained previously, resulting in the maximum error rate in the yield of 3%.

There are several other works that have built approximate models regarding the SPICE simulations taking into account the MCA in the loop
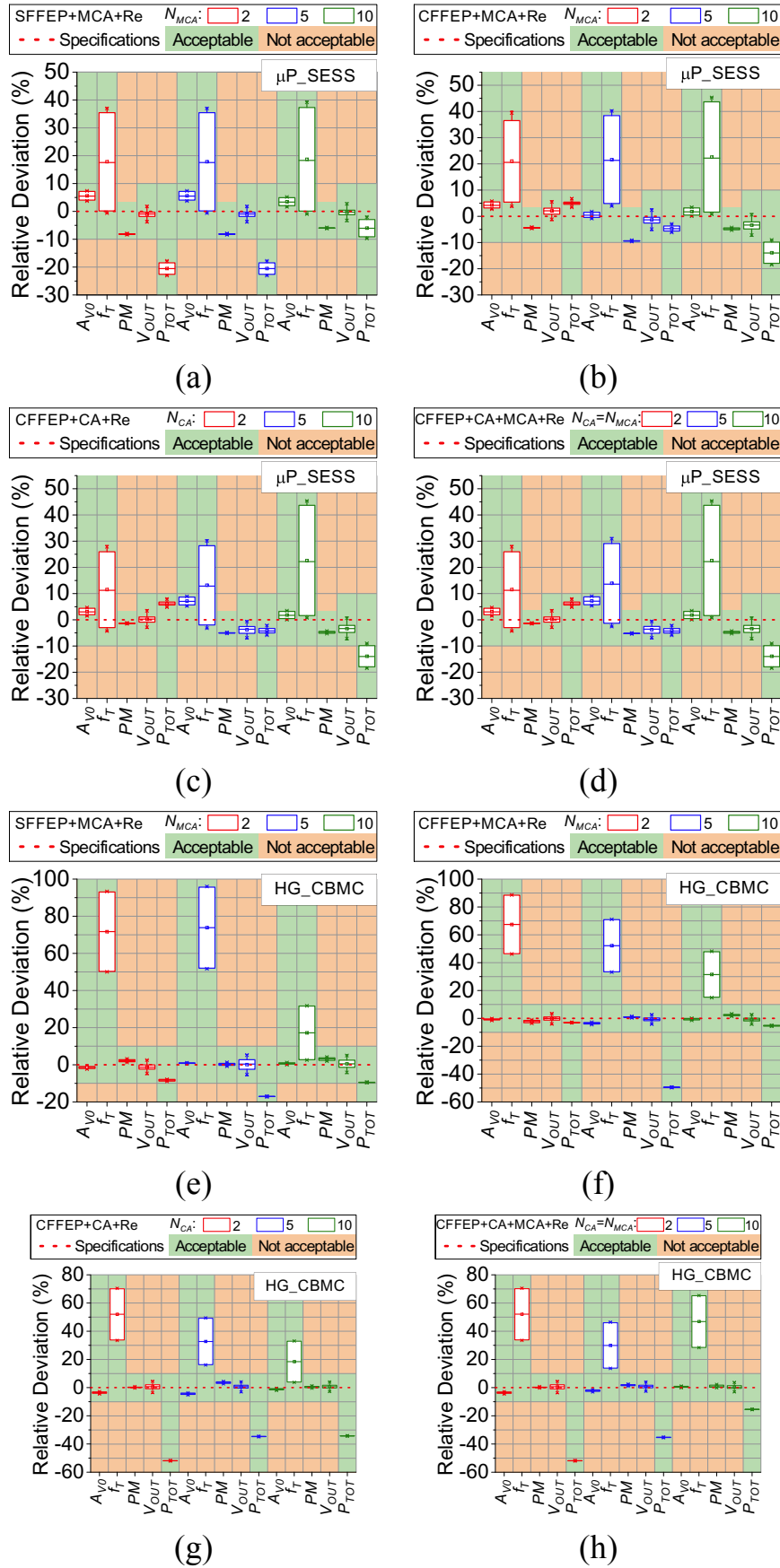
Fig. 4. The relative deviations in percentage of each FoM in relation to their desired specifications (box plots), which were obtained from the SS_{MCA} of the most robust potential solutions of the µP_SESS and HG_CBMC OTAs, regarding the different GA evolution processes implemented in the MTGSPICE.

of the optimization process to subsequently be used to predict the variability effects in analog CMOS ICs (metamodeling techniques). The authors of [3] proposed the Kriging technique to implement metamodels for the design of analog CMOS ICs. They replaced the SPICE simulations regarding the MCA with the Kriging metamodel to predict the electrical performance of analog CMOS ICs, considering manufacturing process variations, in order to reduce the optimization cycle time. The proposed technique obtained average errors of 0.7% and 0.33%, respectively, for the two figures of merit considered. Besides, they have improved the optimization time about 10 times in relation to SPICE simulations concerning the MCA. The disadvantages of the model-based approaches are the huge setup time and the difficulty of reusing these metamodels for different analog CMOS ICs and technology nodes [9].

The authors in Ref. [22] presented MOJITO-R, a tool which performs structural synthesis and optimization of analog CMOS ICs, taking into account robustness analysis regarding the manufacturing process variations. This tool applied a model of process variations instead of the traditional MCA. The authors compared their approach with the MCA taking into account a reduced number of samples (30). The robustness analysis used by the proposed tool achieved an optimization cycle time ten times faster than the standard MCA. However, approximated models were applied regarding the manufacturing process variations.

To the best of our knowledge, the most similar works to ours are those described in Refs. [9,21], respectively, which use the conventional MCA in the loop of the optimization process. The approaches used by these references consider the use of different approximation methods (k-means algorithm and hybrid sampling method) to reduce the simulation time during the optimization process. However, the accuracies of these techniques are limited.

2.1. Contributions of this work

The main contributions of this work are the implementation of a customized GA containing the following features: I- the different types of fitness functions (minimization, central value, and maximization) that were implemented in the MTGSPICE [14] were modified to consider the robustness of the potential solutions which are obtained through the SS_{RA} (CA and/or MCA); II- the elitism process considers the most robust potential solutions obtained to execute the crossover and mutation processes; III- application of a reuse approach of the figures of merit (specifications) previously obtained through the SPICE simulations (nominal) and SS_{RA} (CA and/or MCA) of the potential solutions (previous generation), which will be used in the next generations of the evolution process in order to reduce the time of the optimization process; V- limitation of the maximum number of SS_{RA}s by generation to be performed by the evolution process, taking into account the number of robust potential solutions already found.

Regarding all changes implemented in the standard GA, our proposal is able to remarkably reduce the optimization times ranging from 23% to 79% in relation to standard approaches. In addition, a reuse technique of the FoMs is proposed in this work. This methodology uses the FoMs already utilized in previous generations to compose a new generation to continue the evolution process of the analog CMOS ICs. Regarding four different experiment conditions [standard fitness function and elitism (SFFE) with the MCA (SFFE + MCA), customized fitness function and elitism (CFFE) with the MCA (CFFE + MCA), CFFE with the CA (CFFE + CA), and CFFE with the CA plus MCA (CFFE + CA + MCA)] considered in this study, the average optimization cycle times were reduced by 53%, 45%; 33%, and 22%, respectively.

Moreover, we observed that the method CA plus MCA proposed in this work was able to perform the optimization processes from 17 to 45 times faster than our previous approach described in Ref. [14], in which the MCA is not included in the loop of the optimization process, regarding two case studies with different OTAs. We have also observed that when we use the CA plus MCA analyses in the SPICE simulations, the number of robust potential solutions increases in relation to those

observed by using the previous approach described in Ref. [14]. Consequently, the proposed strategies in this work are remarkably capable of reducing the number of MCAs performed during the optimization processes, favoring the use of the MCA in the loop of the optimization process, without using approximation methods, which usually degrade the accuracy of the robustness study of the analog CMOS ICs. Therefore, our customized GA is able to reduce the optimization process cycle time, without degrading the reliability and accuracy of the robustness study of the analog CMOS ICs design.

3. The robustness driven optimization process

This section describes a novel robustness driven optimization process implemented in an evolutionary system to optimize analog CMOS ICs, named MTGSPICE. MTGSPICE, developed in visual C++ language, integrates the Spice Opus simulator [23] and incorporates the innovative non-linear fitness functions proposed in Ref. [14]. Aiming to improve the effectiveness of the optimization process and robustness (tolerance to the variations to the manufacturing process and environmental conditions) of the analog CMOS ICs designs, this computational tool is capable of performing the optimization process by using the GA with the in-loop RA regarding three different ways: I- *executing the CA*; II- *executing the MCA*, and III- *executing both the CA and MCA*, in which the CAs are performed first, and subsequently, the MCAs are performed only for those potential solutions which met all desired specifications found by the CAs. The flowchart of the customized GA concerning the SS_{RA} (CA and/or MCA) in the loop of the optimization process is illustrated in Fig. 1.

Block A of the flowchart of Fig. 1 is responsible for the configuration of MTGSPICE according to Refs. [14,24]. The designer must provide 1) the SPICE *netlist* [input file containing the description of the analog CMOS IC, MOSFETs dimensions (channel length, L, and channel width, W), the drain current (I_{POL}) and the common-mode input voltage (V_{POL}) of the differential pair, and the technological parameters of the CMOS ICs manufacturing process, which are the input design variables]; 2) the desired specifications [open loop voltage gain (A_{V0}); unit voltage gain frequency (f_T); phase margin (PM); DC output voltage (V_{OUT}); power consumption (P_{TOT}); and total gate area of MOSFETs (A_G), which are the output variables] with their respective tolerance ranges; 3) the GA parameters [N_{CA} and N_{MCA}, which are the number of robust potential solutions to be found in the optimization process through SPICE simulations considering the CA and MCA, respectively, which are new GA parameters implemented in this new MTGSPICE version; N_{Iter} is the maximum number of generations to be evolved (stop criterion if N_{CA} and/or N_{MCA} is not found); N_P represents the population size; P_C and P_M are the crossover and mutation rates, respectively; We_i are the weights of each FoM of the fitness function, in which i is the index that represents each FoM; and σ is the standard deviation of the Gaussian-based fitness functions [14]]. Besides, we must configure the minimum and maximum values of L and W of the MOSFETs and I_{POL} and V_{POL} of the differential pair of the OTA. In addition, if the Miller OTA is being designed, the minimum and maximum values of the Miller capacitance (C_f) must be configured.

MTGSPICE performs a non-conventional evolution process, which is performed in two stages. A more detailed flowchart of this computational tool can be found in Ref. [24]. The first stage, named DC evolution process and illustrated in Block B in Fig. 1, is responsible for evolving the bias conditions of the MOSFETs to ensure that all operate in the desired operation region, e.g. saturation region, and also meet the specifications of the DC bias conditions of the analog CMOS IC, such as V_{OUT}, P_{TOT}, and A_G. In the end of the DC evolution process, N_{CA} or N_{MCA} potential solutions are found, which meet the DC desired specifications of the analog CMOS IC.

Posteriorly, the second stage of the evolution process of the MGTSPICE, named AC evolution process, is started (Block C in Fig. 1). Firstly, a population is randomly generated with N_P potential solutions. Secondly, the potential solutions found in the DC evolution process must

randomly replace potential solutions (defined by N_{CA} and N_{MCA}), which were created randomly in this second stage of the evolution process.

Block D of Fig. 1 is responsible for avoiding repeated potential solutions. If this occurs, they are replaced by other which are generated randomly. This step is important to better explore the search space of the potential solutions and consequently to always obtain different robust potential solutions.

Next, the evolutionary system of the MTGSPICE activates the execution of the SPICE simulations of the current generation (Block E of Fig. 1). These simulations are responsible for obtaining the FoMs of the analog CMOS IC (nominal desired specifications: A_{V0}, f_T, PM, V_{OUT}, P_{TOT}, and A_G). It is important to highlight that each potential solution of a specific population is related to its FoMs (desired specifications), which are obtained through the SPICE simulations. The FoMs and the design variables (dimensions and bias conditions of the MOSFETs) of these potential solutions are stored in memory. Knowing that the next generation of the GA always contains at least the best potential solution evaluated of the previous generation to ensure that the evolution process continues, its SPICE simulation is not performed again (reuse strategy of the potential solutions previously found) to avoid waste of time.

Block F of Fig. 1 is responsible for calculating the value of the fitness function [*Eval(FoM$_i$)*: from 0 (out of specification) to 100 (fully meets the desired specification)] of each FoM found, depending on the profile considered for the fitness function (minimization, center value, and maximization) [14], according to (1).

$$Eval(FoM_i) = 100 \, exp\left(-\frac{\varepsilon_{Typ(i)}^2}{2\,\sigma^2}\right), \tag{1}$$

i is the index of the FoM; σ represents the standard deviation of the Gaussian fitness function (defined by the designer), and $\varepsilon_{Typ(i)}$ is the relative error of the FoM found through the SPICE simulation in relation to the desired specification, given by (2):

$$\varepsilon_{Typ(i)} = \frac{Perf_{Typ(i)} - Spec_{(i)}}{Spec_{(i)}}, \tag{2}$$

where $Perf_{Typ(i)}$ represents the nominal value of the FoM found through the SPICE simulation; $Spec_{(i)}$ represents the desired value of the specification.

The value of the fitness function of a potential solution (*Eval$_{Sol}$*) [equation (3)] taking into account all FoMs found, aiming to meet all desired specifications, is calculated by the weighted sum considering the values of the FoMs and their corresponding weights (*We$_i$*), which are defined by the designer [14].

$$Eval_{Sol} = \sum_{i=1}^{N_{FoM}} Eval(FoM_i) \, We_i, \tag{3}$$

where N_{FoM} is the total number of evaluated FoMs.

After all potential solutions are evaluated by (3), they are sorted from the highest to the smallest fitness function values. Next, the potential solution with the highest value of the fitness function will be used to compose the next generation to ensure the continuation of the evolution process.

Block G of Fig. 1 is responsible for verifying whether there are potential solutions that meet all desired specifications simultaneously. If they exist, MTGSPICE triggers the SS$_{RA}$ (*only CA*, *only MCA*, or both *CA plus MCA*) of these potential solutions which are the best evaluated by the fitness function given by (3), limited by N_{CA} or N_{MCA}, as shown in Block H. The minimum and maximum FoMs values and the design variables (dimensions and bias conditions of the MOSFETs) of these potential solutions are also stored in memory. The objective is to avoid the performing of repeated SS$_{RAs}$ in the future, if any potential solution of the previous generation is used to compose the next generation. This reuse strategy is frequently used by our proposal because the evolution process

of the GA always takes into account either the best evaluated potential solution(s) (while MTGSPICE does not find one robust potential solution) or the most robust potential solution(s) found in the previous generation(s) evaluated. It is important to emphasize that in this work, all individuals (potential solutions) of the population that were not previously evaluated are stored in computer memory along with their corresponding performances (*W*, *L*, bias conditions, figures of merit and robustness obtained by SPICE simulations) in which the user can limit the number of stored solutions in order to save memory space.

Regarding Block I of Fig. 1, it is responsible for verifying if the maximum and minimum FoM values obtained through the SS$_{RA}$ are between the maximum and minimum specifications values. Posteriorly, MTGSPICE calculates the quantity of robust potential solutions. If robust potential solutions do not exist, MTGSPICE calculates the relative errors of each FoM of each potential solution which is obtained through the SS$_{RA}$. The relative errors are calculated depending on the profile type of the fitness function (central value, minimization, and maximization [14]): I- "central value": as this specification is defined by the minimum, nominal, maximum values, two errors are calculated. The first (second) one is calculated considering the maximum (minimum) FoM value subtracted from the nominal desired specification; II- "maximization": as this specification is defined by only one value (value of the desired minimum specification); III- "minimization": as this specification is defined by only one value (value of the desired maximum specification). Besides, in the case of the "central value" profile of the fitness function, the relative error considered for the FoM [$\varepsilon_{WC(i)}$] is the one that presents the highest value between the two relative errors found. Subsequently, MTGSPICE calculates the value of a new fitness function which takes into account these relative errors [*Eval(FoM)'*]. This is done to penalize the FoMs of the potential solutions found that present the highest relative errors, according to (4), to reduce the chance of the least robust potential solutions being chosen to compose the next generation of the GA evolution process (selection, crossover, and mutation).

$$Eval(FoM_i)' = 100 \, exp\left(-\frac{\varepsilon_{WC(i)}^2}{2\,\sigma^2}\right), \tag{4}$$

Afterwards, the values of the fitness functions regarding these non-robust potential solutions (*Eval$_{Sol}$*) are recalculated by (3) to be considered in the robustness driven elitism process.

If there is at least one robust potential solution, the relative errors of each FoM are calculated following the same procedure described for the non-robust solutions. In addition, the robustness value of the robust potential solutions (ε_{PS}) is calculated. It is obtained through the average value of the relative errors of the robust potential solutions taking into account the minimum and maximum values of each FoM in relation to the desired specifications. The higher this error, the worse is the value of its robustness. This is done aiming to perform the ranking of the best robust potential solutions which must be provided to the designer, depending on the values of N_{CA} and/or N_{MCA}. If the total number of robust potential solutions is not achieved, which is defined by N_{CA} and/or N_{MCA}, MTGSPICE saves the robust potential solutions found so far to be used to compose the next generation through the elitism, selection, crossover, and mutation processes (Block J of Fig. 1). If we have more than N_{CA} and/or N_{MCA} robust potential solutions, they are resorted from the smallest to the highest robustness value (ε_{PS}) and the most robust potential solutions are provided to the designer.

Block K of Fig. 1 performs the innovative robustness driven elitism process. If the RAs (*only CA*, *only MCA*, or both *CA plus MCA*) are not selected in the MTGSPICE by the designer, the elitism process to be performed is the standard one, i.e. the best potential solution (which presents the highest value of the fitness function) is selected to continue the GA evolution process. If the *only CA* method is selected, the potential solutions that present the highest robustness (smallest ε_{PS}) are selected to continue the GA evolution process, in which the maximum number of robust solutions to be found is limited by the N_{CA} parameter. If the *only*

MCA method is selected, the potential solutions that present the highest robustness are designated to continue the GA evolution process, in which the maximum number of robust solutions to be found is limited by the N_{MCA}. If the *CA plus MCA* method is selected, the potential solutions that present the highest robustness values of the MCA are selected to continue the evolution process, where the maximum number of robust solutions to be found is limited by the N_{MCA}, due to the MCA is more accurate than the CA.

However, if a potential solution is robust only by the CA and it is not robust by the MCA, the elitism process considers the robust potential solutions by the CA during the optimization process until it meets the robustness regarding both methods (*CA plus MCA*). Afterwards, the population is reordered from the highest to smallest fitness function values (*Eval_Sol*). Subsequently, the most robust potential solutions found by one of these methods (*CA*, *MCA*, or *CA plus MCA*) must replace the potential solutions of the current generation that present the smallest values of fitness functions. In the case of the *CA plus MCA* method, the most robust potential solutions found through the MCA must replace the potential solutions of the current generation that present the smallest values of fitness functions. Then, the current population is reordered, in which the value of the fitness function of each individual is changed taking into account its robustness. On the other hand, if there are no robust solutions previously saved, then the solution that presented the highest value of the fitness function in the population, before the RAs, is identified. If the fitness function value *EvalSol*, obtained by (3), was downgraded through the fitness function driven by robustness in (4), then the original fitness function value is restored. This is done to avoid a stagnation of the evolution process while there are no robust solutions.

In Block L of Fig. 1, the input variables (*L*, *W*, bias conditions of the MOSFETs), FoMs (A_{V0}, f_T, *PM*, etc.) of the CMOS IC and the value of the fitness function (*Eval_Sol*) of the best robust potential solution are saved in a data log and plotted on graphics, in real time, allowing the designer to observe how the optimization process happens to meet the desired specifications. Fig. 2 shows the monitoring of the value of the fitness function of the best robust potential solution, FoMs found by the MTGSPICE, taking into account the CA and/or MCA in the loop of the optimization process as a function of the number of iterations.

Block M of Fig. 1 is responsible for performing the selection (binary tournament [13]), crossover (single-point crossover [13]), and bit flip mutation [13] genetic operators in the current generation to create a new generation to be optimized.

Block N of Fig. 1 is responsible for stopping the GA optimization process by verifying if the N_{CA} or N_{MCA} robust potential solutions are found or the maximum number of iterations (N_{Iter}) is reached. If these two conditions are not reached, a new generation is optimized.

Block O in Fig. 1 is responsible for providing the potential solutions found through the GA optimization process.

4. CMOS OTAs' topologies

Fig. 3 illustrates the electrical circuits of the topologies of two CMOS OTAs used in this work. The first one, Fig. 3(a), is a single-ended single-stage OTA (SESS) [25]. We have chosen this topology because it is an important basic analog building block that is applied in a wide variety of analog CMOS ICs applications, such as voltage gain amplifiers, comparators, data recovery circuits in radio frequency (RF) identification devices, voltage-controlled oscillators, optical transceivers, and filters [14]. The second one, illustrated in Fig. 3(b), is the cascoded-bias Miller--compensated OTA (CBMC) [26], which is also a basic building block widely used in analog electronics [14,26].

In Fig. 3(a), C_L is the capacitive load, V_{DD} and V_{SS} are the positive and negative voltages of the symmetrical supply, respectively, V_{OUT} is the OTA output voltage, v_{I+} and v_{I-} are the non-inverting and inverting input voltages of the OTA, respectively, I_{POL} is the current source of the differential pair of the OTA, M3 and M5 and also M4 and M6 are pMOSFETs, which work as current mirrors, and M7 and M8 are nMOSFETs that also

operate as current mirrors. Besides, the pairs of MOSFETs M1-M2, M3-M4, M5-M6, and M7-M8 are matched, but M9 and M10 are not necessarily matched aiming to obtain a better current mirroring [14]. In the designs of these two OTAs, we consider that the MOSFETs' channel lengths (*L*) of the current mirrors present the same value for the proper matching of the V_{th} regarding the MOSFETs in the current mirror configuration [14]. In Fig. 3(b), M1 and M2 are nMOSFETs (matched differential pair), M3 and M4 are pMOSFETs (matched active loads of the differential stage working in the current mirror configuration), M5 is a pMOSFET, and M11 is an nMOSFET which composes the output stage (second stage). M6, M7, and M8 are also nMOSFETs in cascode configuration operating as current mirrors [26]. The nMOSFET pairs M9-M10 and M9-M11 operate as current mirrors biasing the first and the second stage, respectively. They are not necessarily matched in this work; however, they have the same *L* [14]. Additionally, C_f is the compensation capacitance which is electrically connected between the first and second stages, adjusted to obtain the desired phase margin [26].

5. OTAs' specifications and configuration parameters of MTGSPICE

The design specifications of the SESS [25] and CBMC [26] OTAs are presented in Table 1. The specifications regarding the SESS were adapted from the Silicon-On-Insulator (SOI) technology, however, they were obtained experimentally by SPICE simulations regarding robust potential solutions with the use of a different CMOS IC manufacturing process (Bulk technology).

In Table 1, µP_SESS means that the SESS OTA operates in micropower bias conditions and HG_CBMC means that the CBMC operates with high voltage gain in ultra-low power bias conditions. In addition, six different specifications are taken into account for these OTAs: A_{V0}, f_T, *PM*, V_{OUT}, P_{TOT}, and A_G. This experiment considers the tolerances of the desired specifications to be equal to ±10%, except the *PM* of the SESS OTA, whose lower limit is set to −10% and the upper limit to +3.45%, due to the maximum typical value adopted for the *PM* to be 90° [25]. The designer can set the minimum, nominal, and maximum values of the desired specifications. This additional feature implemented in the MTGSPICE is intended to help non-expert designers to find robust potential solutions in practice as close to feasible specifications as possible. Consequently, these designers can better specify an analog CMOS IC to be used in a project, change the architecture of the circuit, choose a more sophisticated manufacturing process to implement it, etc.

Moreover, in these designs of the OTAs, all transistors must operate in the saturation region (functional constraints). The capacitive load (C_L) is adopted to be equal to 15 pF (µP_SESS) and 1 pF (HG_CBMC), respectively. Additionally, the symmetric supply voltages (V_{DD} and V_{SS}) applied to the µP_SESS and HG_CBMC OTAs are ± 1.25 V and ±0.5 V, respectively, and their operating temperatures are considered to be equal to 27 °C. The Bulk CMOS ICs manufacturing processes used to implement the µP_SESS and HG_CBMC OTAs are respectively 350 nm from the ON Semiconductor and 130 nm Silicon–Germanium (SiGe) from Globalfoundries (IBM) [27].

5.1. Optimization parameters of the OTAs

Table 2 presents the ranges of values adopted for the optimization parameters related to the MOSFETs' dimensions (minimum, maximum, and step size values) to perform the evolution processes of the µP_SESS and HG_CBMC OTAs, respectively. These values were defined by the designers regarding their previous knowledge and experiences in analog CMOS ICs designs. Furthermore, the parameters regarding the geometric variables [channel length (*L*) and width (*W*)] of the MOSFETs were set to present dimensions which are proportional to the grid of the design rules of the CMOS ICs technologies used in each OTA design, aiming to facilitate their layouts' implementations.

5.2. Fitness functions parameter settings

The default values for the weights (We_i) of the GA fitness function for all OTA FoMs (desired specifications) were considered the same to perform the DC evolution process, i.e. 33.3% for V_{OUT}, P_{TOT}, and A_G. Similarly, regarding the AC evolution process, we have considered the same weights (16.7%) for the FoMs (A_{V0}, f_T, PM, V_{OUT}, P_{TOT}, and A_G). These weights can be redefined by the designers. It is important to highlight that our recommendation for the designers is to consider the weights with the same values (default values) [14]; however, if robust potential solutions are not found through the GA optimization process, the designer can change them during the evolution process to facilitate the analog CMOS ICs optimization.

5.3. DC evolution process parameters considered

The population sizes (N_P) were set to be equal to 20 and 30, respectively, for the µP_SESS and HG_CBMC OTAs. N_{Iter} (maximum number of generations to be evaluated) was set to be equal to 5000. The σ parameter of the Gaussian fitness function was set to 0.08 for all profiles considered (minimization, maximization, and central value), which is related to a maximum tolerance of 10% for the desired specifications (figures of merit of the OTAs) [14]. Two new parameters were added to the MTGSPICE, named N_{CA} and N_{MCA}. The N_{CA} represents the number of desired robust potential solutions by the designer, which is obtained through the SPICE simulations regarding the DC analysis with the CA. The N_{MCA} is similar to the N_{CA}, but it is related to the MCA. If the number of desired robust potential solutions, given by N_{CA} and/or N_{MCA}, is obtained before the N_{iter} is reached, the GA optimization process is ended. The number of runs (N_R) parameter was set to be equal to 1. This means that in the end of the DC evolution process, we have obtained N_{CA} or N_{MCA} DC robust potential solutions.

Besides, it is important to emphasize that after the DC optimization process is ended, the best DC potential solutions, given by N_{CA} or N_{MCA}, are used to compose the initial population to perform the AC evolution process of the OTAs.

5.4. AC evolution process parameters

The population sizes (N_P) were set to be equal to 50 and 100, respectively, for the µP_SESS and HG_CBMC OTAs. The N_{Iter} value was set to be equal to 5000 for both designs of the OTAs. The σ parameter regarding the fitness functions is set to 0.08 [14]. In order to obtain a higher number of robust potential solutions, the N_R parameter was set to be equal to 10 for both OTAs. For each run, a different seed is considered for the random generator used by the optimization process, which corresponds to the different initial populations (sets of individuals or chromosomes, which represent the dimensional parameters and bias conditions of MOSFETs). At the end of the AC evolution process, we obtained 10 (N_R) multiplied by N_{CA} or N_{MCA} robust potential solutions (for example, if $N_R = 10$ and $N_{CA}=N_{MCA}=2$, we would have 20 robust potential solutions). However, from these 10 (N_R) multiplied by N_{CA} or N_{MCA} robust potential solutions, we would only consider the N_{CA} or N_{MCA} best robust potential solutions obtained. Besides, the single-point crossover was applied with a probability (P_C) of 0.7, and the mutation probability (P_M) is set to 0.03 [14].

5.5. CA and MCA parameters

Regarding the SS_{CA}, we have considered 3σ variations related to the CMOS ICs manufacturing processes used to perform this work, taking into account the threshold voltages (V_{th}) and mobility of the charge carriers along the channel length (μ_0) of MOSFETs, where the 0 in μ_0 can be considered n for electrons or p for holes. These parameters are responsible for affecting the main analog parameters of the MOSFETs, such as the transconductance (g_m). The extreme global variations of V_{th}

and μ_0 were set to $\pm10\%$ and $\pm6\%$, respectively, for the nMOSFETs, and $\pm12\%$ and $\pm10\%$, respectively, for the pMOSFETs [28]. Therefore, the extreme operating conditions of the nMOSFETs and pMOSFETs were considered during the CA. In the operating condition named *Fast-Fast*, the nMOSFETs and pMOSFETs operate at the maximal g_m. In the operating condition named *Slow-Slow*, the nMOSFETs and pMOSFETs operate at the minimal g_m. In the operating condition named *Fast-Slow*, the nMOSFETs operate at the maximal g_m and the pMOSFETs at minimal g_m. Finally, in the operating condition named *Slow-Fast*, the nMOSFETs operate at the minimal g_m and the pMOSFETs at maximal g_m. In addition, the lowest value of the V_{th} and the highest value of μ_0 define the maximal g_m, and the highest value of the V_{th} and the lowest value of μ_0 define the minimal g_m regarding the nMOSFETs and pMOSFETs. Besides the four operating conditions (*Fast-Fast*, *Slow-Slow*, *Fast-Slow*, and *Slow-Fast*), environmental variations were also considered. Therefore, two temperatures, 0 °C and 75 °C, were considered for each operating condition, totalizing eight combinations.

The SS_{MCA} takes into account the local and global variations of the V_{th} and μ_0 (considering Gaussian profiles) and temperature [25]. As we considered 50 global variations (N_{GLob}), 50 local variations (N_{Loc}), and two different temperatures (0 °C and 75 °C), each SS_{MCA} has performed 5000 MCA analyses ($N_{GLob}\cdot N_{Loc}\cdot2$). The standard deviations of the V_{th} and μ_0 global variations were set to $\pm3.3\%$ and $\pm2\%$, respectively, for the nMOSFETs, and $\pm4\%$ and $\pm3.3\%$, respectively, for the pMOSFETs [28]. Besides, the standard deviations considered for the V_{th} (σ_{M_Vth}) and μ_0 ($\sigma_{M\_\mu0}$), due to the local mismatches between the MOSFETs, are given by $A_{Vth}/\sqrt{2\,WL}$ and $A_{\mu0}/\sqrt{2\,WL}$, respectively, where A_{Vth} and $A_{\mu0}$ represent the proportionality constants of the V_{th} and μ_0, which are obtained experimentally [28]. The A_{Vth} and $A_{\mu0}$ parameters used for the nMOSFETs are 5×10^{-3} V µm and 1.04×10^{-2} µm, respectively, and 5.49×10^{-3} V µm and 0.99×10^{-2} µm for the pMOSFETs [28].

In this work, we have considered only the default parameters that are considered in SPICE Opus simulator to perform the Monte Carlo analyses. However, the designers can consider in their simulations all parameters of the manufacturing process which can be important to design the CMOS IC. To do this it is necessary that designers add the other parameters in the input file (netlist) of the IC optimized by the MTGSPICE. The cycle time of the optimization process depends on the number of the parameters considered in the robustness analyses (Corner and Monte Carlo).

6. Results

MTGSPICE was run in a 3.4 GHz IBM-PC with 24 GB RAM and Windows 10 (operating system). The experiments of this work were performed concerning three different robustness conditions: I) taking into account the SPICE simulations regarding AC analysis with the CA (SS_{CA}); II) taking into account the SPICE simulations regarding AC analysis with the MCA (SS_{MCA}); and III) taking into account the SPICE simulations regarding AC analysis with the CA plus MCA (SS_{CA+MCA}). For each robustness condition, we have configured MTGSPICE under three different optimization process conditions using the customized fitness function, which degrades the value of the fitness function of the potential solutions that present one or more FoMs out of the desired tolerance range of the desired specification. Moreover, the robust elitism considers the most robust potential solutions obtained to execute the crossover and mutation (CFFE): I) The N_{CA} was set to be equal to 2, 5, and 10, respectively, aiming to obtain two, five, and ten robust potential solutions by performing the SS_{CA}; II) The N_{MCA} was set to be equal to 2, 5, and 10, aiming to obtain two, five, and ten robust potential solutions by performing the SS_{MCA}; III) The N_{CA} and N_{MCA} were set to be equal to 2, 5, and 10, which have obtained two, five, and ten robust potential solutions by performing the SS_{CA+MCA}. It is important to emphasize that the N_{CA} and N_{MCA} were configured to present the same values regarding the optimization processes performed in this work (DC and AC evolution processes).

Furthermore, another experiment was carried out for comparison purposes with the experiments previously described, considering the standard evolution process with the GA, taking into account the SS_{MCA} in the optimization loop. In order to perform this study, we used MTGSPICE, but the DC evolution process was not applied, the non-robust potential solutions by performing the SS_{MCA} were not penalized by the use of the fitness function driven by robustness (Block I of Fig. 1), and the robustness driven elitism (Block K of Fig. 1) was not used (the conventional elitism was applied), where only the potential solution that presented the highest value of the fitness function in each generation of the GA was selected as the best potential solution to be used in the next generation of the evolution process. Therefore, this optimization condition will be identified as the standard fitness function and elitism (SFFE). This experiment considers the use of the following settings: N_{MCA} was set to be equal to 2, 5, and 10, which are responsible for obtaining two, five, and ten final robust potential solutions.

Additionally, we have performed ten runs ($N_R = 10$) regarding ten different seeds, which were generated randomly, for each one of the three different conditions for the robustness analyses to be performed (SS_{CA}, SS_{MCA}, and SS_{CA+MCA}). However, to reduce the stochastic differences due to the use of different random seeds in these experiments, we used the same set of ten seeds for each robustness analysis (with the CA, MCA, and CA plus MCA). At the end of these AC evolution processes regarding the robustness analyses, we have 10 multiplied by N_{CA} or 10 multiplied by N_{MCA} robust potential solutions, in which N_{CA} or N_{MCA} potential solutions are obtained from each optimization run. Therefore, to perform the experiments in this work, we have selected only the best robust potential solutions (smallest ε_{PS}) that were obtained through the SS_{CA}, SS_{MCA}, and SS_{CA+MCA}, respectively, considering each optimization run.

6.1. Design optimization cycle times of the OTAs

The objective of this first analysis is to evaluate the optimization cycle times (OCTs) of the designs of two different OTAs taking into account three different robustness analyses (CA, MCA, and CA plus MCA), two different evolution processes, SFFE and CFFE, and by using the reuse strategy (Re) of the FoMs (A_{V0}, f_T, PM, etc.) obtained through the SPICE simulations regarding the AC analysis with RAs of the potential solutions in the previous generation that are used in the next generation to continue the GA evolution process. Table 3 presents the average values and standard deviations in percentage [SD (%)] of the OCTs in minutes, considering different N_{CA} and/or N_{MCA} (2, 5 and 10), ten different runs, two different OTAs (μP_SESS and HG_CBMC), without and with the utilization of the reuse strategy, respectively, and two different evolution processes have been considered in this study. These studies were classified as: I- Use of the SFFE of the GA by using the SS_{MCA} (indicated by SFFE + MCA); II- Use of the CFFE of the GA by using the SS_{MCA} (indicated by CFFE + MCA); III- Use of the CFFE of the GA by using the SS_{CA} (indicated by CFFE + CA); IV- Use of the CFFE by using the SS_{CA+MCA} (indicated by CFFE + CA + MCA). All these studies were also performed considering the reuse strategy, indicated by "Re" in Table 3.

By analyzing Table 3, regarding the μP_SESS and HG_CBMC designs, with and without the application of the reuse strategy, we observe that by increasing the number of robust potential solutions, the OCT also increases, concerning the MCA (SFFE + MCA and CFFE + MCA for N_{MCA} equal to 2, 5, and 10). This fact can be justified due to a higher number of SS_{MCA} that must be performed to reach the desired specification. Moreover, the same results also can be seen regarding CFFE + CA for N_{CA} equal to 5 and 10 for both OTAs and also CFFE + CA + MCA for N_{CA} and N_{MCA} equal to 5 and 10 for the μP_SESS design. However, these results are not observed for the CFFE + CA for N_{CA} equal to 2 and CFFE + CA + MCA for N_{CA} and N_{MCA} equal to 2. This can be explained because although the CA is faster than the MCA, it is strongly impaired by the use of a smaller number of robust DC potential solutions to compose the initial generation (population) to be evolved by the AC evolution process (for instance: the

design OCT regarding the CFFE + CA for N_{CA} equal to 2 is almost double than the CFFE + CA for N_{CA} equal to 5, for both OTAs designs). Besides, this can also happen because of the feature of the CFFE + CA to consider the most limiting operating conditions of MOSFETs. It is important to note that the CFFE + CA + MCA for N_{CA} and N_{MCA} equal to 2, 5, and 10, regarding the HG_CBMC design, presents an inverse trend to the cases analyzed before as the OCTs are reduced. This occurs because the innovative robustness driven elitism process exploits the most robust potential solutions found during the optimization process to find other new potential solutions to compose the next generations through the crossover and mutation processes.

Additionally, the standard deviations of the results obtained in this study are usually high (greater than 20%). This can be explained because the GA evolution process depends on the initial population (generation), which is randomly generated. Besides, we can also observe that only the optimization process regarding the CFFE + CA + MCA for N_{CA} and N_{MCA} equal to 10 presents the smallest values of the standard deviations (about 25%) for both μP_SESS and HG_CBMC OTA designs. This happens because it uses a higher number of robust DC potential solutions (10 in this case), i.e. a smaller number of potential solutions created randomly than the others (2 and 5) to compose its initial population. It also uses a higher number of robust potential solutions in its robustness driven elitism and, consequently, in the crossover and mutation processes.

Considering the μP_SESS OTA studied, we observed that the reuse technique, regarding all the robustness analyses considered (SFFE + MCA, CFFE + MCA, CFFE + CA, and CFFE + CA + MCA), is capable of reducing the average OCTs by approximately 50%, 47%, 32%, and 22%, respectively, in comparison to the analyses performed without considering the reuse strategy. Furthermore, we observed that the reduction of the average OCTs regarding the HG_CBMC design follows the same trend of those observed in the μP_SESS design (56%, 43%, 33%, and 21%), when we use the reuse strategy. Therefore, we also conclude that the reuse strategy of the FoMs already obtained through the SPICE simulations considering the AC analysis with robustness analyses of previous generations in the evolution process of the next generations is able to remarkably reduce the OCTs of the OTAs' designs, especially for the optimization processes that consider the MCA. Moreover, the reuse strategy applied for the CFFE + CA + MCA approach presents a smaller capability to reduce the OCTs of the OTAs' designs in relation to the other approaches performed by only using the Monte Carlo or corner analyses. This occurs because it is already able to reduce the OCTs due to it integrates an innovative customized fitness function which considers the robustness of the potential solutions found, a new elitism process which takes into account the most robust potential solutions to generate the next generations to continue the evolution process and use the most robust potential solutions found in the SS_{CA} to compose the next generations to be evolved by using the SS_{MCA} and consequently reducing the benefits of the reuse strategy.

Another important result that we have observed is that the novel approaches proposed by this work (CFFE and the use of the MCA and the CA + MCA, without or with the reuse strategy) also are able to reduce the OCT by 37% (CFFE + MCA), 33% (CFFE + MCA + Re), 79% (CFFE + CA + MCA), and 68% (CFFE + CA + MCA + Re) respectively, regarding the μP_SESS design, and 44% (CFFE + MCA), 26% (CFFE + MCA + Re), 68% (CFFE + CA + MCA), and 43% (CFFE + CA + MCA + Re), respectively, considering the HG_CBMC design, in relation to the SFFE with the use of the MCA without the reuse strategy (SFFE + MCA) and with the reuse strategy (SFFE + MCA + Re).

Furthermore, considering the approaches that use the SS_{MCA} in the loop of the optimization process (SFFE + MCA, CFFE + MCA, and CFFE + CA + MCA, with and without the reuse strategy), the fastest are the CFFE + CA + MCA and CFFE + CA + MCA + Re. This can be explained as these approaches use the SS_{CA} initially to find some robust potential solutions which are posteriorly used to perform the evolution process through the SS_{MCA}. This customized approach between these two RAs (CA and MCA) proposed by our work was capable of reducing the

average OCT by 79%, 68%, 67%, and 52%, respectively, in relation to the SFFE + MCA and CFFE + MCA, with and without the reuse strategy, regarding the μP_SESS design, and by 68%, 43%, 44%, and 23%, respectively, considering the HG_CBMC design. In addition, the CFFE + CA + MCA + Re approach presented average OCTs 65% and 16% higher than those found in the CFFE + CA + Re approach, regarding the μP_SESS and HG_CBMC designs, respectively. Our results have been able to reduce the OCTs of the OTAs' designs without impairing the accuracy of the robustness and without reducing the search space of the potential solutions, obtaining similar results in terms of OCTs of an OTA's design, as described by Ref. [9].

Another experiment has been performed to evaluate the effectiveness of the customized GA optimization process with in-loop CA plus MCA (CFFE + CA + MCA + Re indicated in Table 4) proposed in this work in relation to that described in Ref. [14]. Ref. [14] considered the GA and the Gaussian profile for the fitness functions, in which 30 optimization runs were performed using Spice simulations without in-loop MCA. The robustness analyses with the MCAs were performed considering those with the highest values of the fitness function, regarding each run ($N_R = 30$). Table 4 presents the average OCTs regarding the CFFE + CA + MCA + Re ($N_{CA}=N_{MCA}=10$) approach and average OCTs obtained by using the approach in Ref. [14] for the μP_SESS and HG_CBMC OTAs' designs. Besides, the number of robust solutions (N° Sol.) obtained after the MCA is also presented.

Analyzing Table 4, considering the μP_SESS and HG_CBMC OTAs, we have observed that the OCTs obtained through the innovative CFFE + CA + MCA + Re approach were respectively 45 and 17 times faster than those found by using the approach of ref. [14]. Furthermore, it is important to observe that the CFFE + CA + MCA + Re approach also has obtained a higher number of robust potential solutions after the RAs with the MCA for both OTAs in relation to those obtained by Ref. [14]. Therefore, this innovative customized GA evolution process proposed in this work, besides being remarkably faster, is also capable of searching and finding a higher number of robust potential solutions than the typical GA evolution process.

6.2. OTAs' robustness

An analog CMOS IC must only be manufactured after the designer performs a detailed and exhaustive study of its robustness, aiming to reduce the risk of malfunction after its manufacture [4]. In order to illustrate the robustness through a box plot of the μP_SESS and HG_CBMC OTAs regarding each approach for the GA evolution process implemented in the MTGSPICE (SFFE + MCA + Re; CFFE + MCA + Re; CFFE + CA + Re; CFFE + CA + MCA + Re), we have considered 10 runs and N_{CA} and/or N_{MCA} equal to 2, 5, and 10. Hence, we have obtained, respectively, 20, 50 and 100 robust potential solutions of each GA evolution process approach. In order to generate the box plot of the robustness of the best potential solution (smallest ε_{PS}) of each OTA, regarding each evolution process approach, we have had to run the SS$_{MCA}$ of these best robust potential solutions to use all results of these simulations (minimum and maximum values of the FoMs due to the variations of the CMOS ICs' manufacturing process and environment conditions). Therefore, Fig. 4 illustrates the relative deviations in percentage of each FoM in relation to their desired specifications (box plots), which were obtained from the SS$_{MCA}$ of the most robust potential solutions of the μP_SESS and HG_CBMC OTAs, regarding the different GA evolution processes implemented in the MTGSPICE.

It is important to highlight that MTGSPICE is able to obtain different solutions. However, the designer can choose any one which best suits his needs taking into account the most desired specifications (A_{V0}, f_T, P_{TOT}, etc.). However, the most important result observed is that all of them were capable of meeting the desired specifications with maximum errors smaller than 10%. Furthermore, we have not included the values of the area regarding the solutions in Fig. 4 because they were not subject to variations in the Monte Carlo analysis. The values of the areas regarding

the four approaches (SFFE + MCA; CFFE + MCA; CFFE + CA; CFFE + CA + MCA) considering N_{CA} and/or N_{MCA} equal to 2, 5, and 10 for the μP_SESS and HG_CBMC OTAs are respectively: 3903; 3903; 3694; 1967; 3373; 6013; 2588; 2364; 6013; 2588; 2375; 6013; 310; 150; 288; 192; 260; 213; 163; 208; 281; 163; 293; 239 (μm^2).

Analyzing Fig. 4, we can see that the yields of all designs of the OTAs are equal to 100% as all GA optimization processes have ensured that the minimum and maximum values of all FoMs obtained through the SS$_{MCA}$ are within the tolerance ranges of the desired specifications (10% in this case, which were set by the designer). Besides, regarding all types of approaches of GA evolution processes and OTAs considered in this study, we can observe that the average relative errors in percentage regarding all FoMs (ε_{PS}) are always smaller than 3.7%. This means that all innovative types of approaches of GA evolution processes are capable of producing similar robust potential solutions in relation to standard GA evolution processes, i.e. they do not degrade the robustness of the potential solutions found.

Furthermore, all these robust potential solutions present maximum standard deviations of the FoMs smaller than 5.2%. This means that the effectiveness of the search by robust potential solutions, regarding all approaches of GA evolution processes, are suitable. Besides, we observe that the robustness of the potential solutions found is only slightly affected (maximum errors smaller than 3.7%) by the number of potential solutions to be found by Corner (N_{CA}) or by Monte Carlo (N_{MCA}) analyses used in these experiments, which were set to 2, 5 and 10, respectively. Similar conclusions were obtained performing the comparison between the CFFE + CA + MCA + Re and that obtained by Ref. [14]. This can be justified due to FoMs set close to their maximum or minimum feasible boundaries of its specifications and the characteristics of a fitness function which is based on a weight sum, which can be improved to further boost the robustness of the potential solutions.

7. Conclusion

This manuscript proposes and qualifies a customized genetic algorithm which incorporates an innovative modified fitness function and elitism process that takes into account the robustness (Corner and Monte Carlo analyses), without degrading the cycle time of the optimization process of the analog CMOS ICs designs. This is achieved by considering only a reduced number of the best robust potential solutions found and without restricting the number of samples of the Monte Carlo analysis. Furthermore, regards the procedure of reuse strategy of the results of the Monte Carlo analysis already obtained previously. We can observe that by using these several approaches, the cycle time of the optimization process of analog CMOS ICs designs can be reduced from 23% to 79% in comparison to the standard optimization process of the GA. Besides, the maximum average error of the figures of merit obtained by the MTGSPICE in relation to the desired specifications of analog ICs was of 3.7%, regarding all optimization processes proposed by this work. Therefore, we can conclude that our customized GA can be considered an alternative strategy to optimize robust analog CMOS ICs that meet the desired specifications and with a cycle time of the optimization process very much reduced (around 1 h).

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